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Letter

Strain-Enhanced Mobility of Monolayer MoS_2

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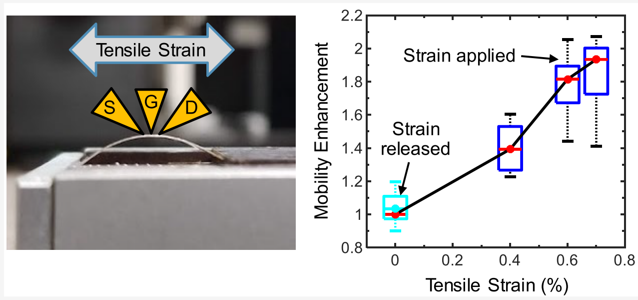

ABSTRACT: Strain engineering is an important method for tuning the properties of semiconductors and has been used to improve the mobility of silicon transistors for several decades. Recently, theoretical studies have predicted that strain can also improve the mobility of two-dimensional (2D) semiconductors, e.g., by reducing intervalley scattering or lowering effective masses. Here, we experimentally show strain-enhanced electron mobility in monolayer MoS_2 transistors with uniaxial tensile strain, on flexible substrates. The on-state current and mobility are nearly doubled with tensile strain up to 0.7%, and devices return to their initial state after release of the strain. We also show a gate-voltage-dependent gauge factor up to 200 for monolayer MoS_2, which is higher than previous values reported for sub-1 nm thin piezoresistive films. These results demonstrate the importance of strain engineering 2D semiconductors for performance enhancements in integrated circuits, or for applications such as flexible strain sensors.

KEYWORDS: *2D materials, MoS_2, transistors, strain engineering, strain sensors, mobility*

Transition metal dichalcogenides (TMDs), a class of two-dimensional (2D) layered materials, have gained interest for electronic and optoelectronic devices due to their atomically thin nature and pristine interfaces that, in theory, lack dangling bonds.[1] Molybdenum disulfide (MoS_2) is a promising TMD because it can be synthesized in single layers,[2,3] it is relatively air-stable,[4] and its band gap is nearly twice that of silicon, which is advantageous for low-power transistors.[1] However, other electrical properties, such as on-state current, mobility, and contact resistance of MoS_2 and other TMD devices must be improved for them to compete with or complement existing technologies based on silicon. Several techniques have been used to experimentally improve TMD-based transistors, such as contact engineering,[5,6] channel doping,[7−9] defect healing,[10] and interface engineering,[11] while strain engineering has been theoretically predicted as an additional method to improve electrical performance.[12−15]

Strain engineering was shown to improve the mobility of silicon metal oxide semiconductor field-effect transistors (MOSFETs) in the 1990s[16,17] and then commercialized with the 90 nm technology node.[18−20] In practice, electron mobility in nMOS silicon FETs is increased by uniaxial tensile strain from silicon nitride encapsulation layers.[19,20] In contrast, higher hole mobility in pMOS silicon FETs is achieved by uniaxial compressive strain imparted by selective growth of SiGe at the source and drain regions.[19,20] Reduced electron effective mass and scattering due to band splitting in the conduction band, and reduced hole effective mass due to band warping in the valence band, lead to enhanced mobility with strain in silicon.[16,19−21] Experimental and theoretical studies have shown that strain can also modify the band structure and phonon dispersion of 2D semiconductors based on TMDs.[12,13,22−24] However, most strained TMD studies to date have focused on optical measurements (e.g., photoluminescence mapping of optical band gap changes with strain[24−26]), and less attention has been paid to strain effects on electron and hole mobility, despite the enhancement predicted theoretically.[12−15]

In this work, we study the effect of uniaxial tensile strain on the electrical performance of monolayer MoS_2 transistors on flexible substrates. We find the mobility and on-state current are nearly doubled with ~0.7% applied strain, reverting to their initial values when the strain is removed. This represents the largest enhancement of TMD mobility with externally applied strain to date, revealing that strain engineering could be just as important as defect- and contact-engineering for enhancing the performance of 2D transistors based on TMDs. We also show that these devices can be used as strain sensors with voltage-dependent gauge factors up to ~200, larger than most conventional strain sensors based on bulk materials and most 2D-based strain sensors.

We fabricate MoS_2 transistors with local back-gates on free-standing polyethylene naphthalate (PEN), a flexible and

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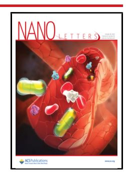

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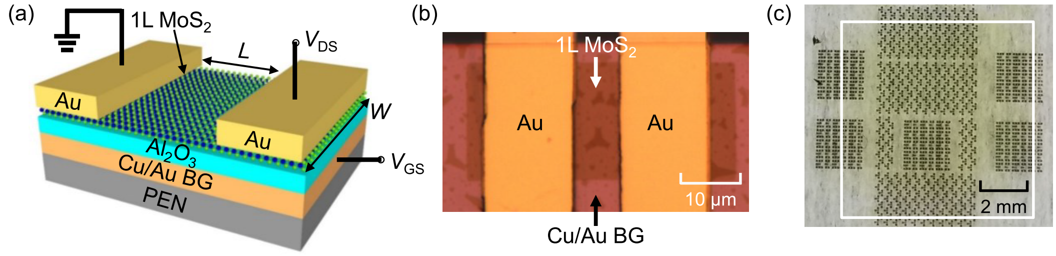

Figure 1. (a) Schematic of back-gated (BG) monolayer (1L) MoS_2 transistor on a polyethylene naphthalate (PEN) flexible substrate, with Au source and drain contacts, and an Al_2O_3 back-gate dielectric ∼20 nm thick. (b) Top-view optical image of 1L MoS_2 device with length L = 8 μm and width W = 20 μm. A few small triangular bilayer regions are visible, but these do not bridge the transistor channel, and we do not expect them to significantly affect the electrical performance of the monolayer MoS_2.[31] (c) Picture of sample (on a cleanroom wipe) taken after fabrication was completed, with the green region within the white box corresponding to the transferred MoS_2 film.

transparent plastic substrate, as shown in Figure 1. The MoS_2 is grown by chemical vapor deposition (CVD) on separate SiO_2/Si substrates,[2] and then transferred[27] onto the Al_2O_3 back-gate dielectric on PEN. We note that monolayer MoS_2 is also a flexible material and can withstand strains up to ∼11%.[28] Detailed steps regarding the fabrication of these transistors are given in Supporting Information Section 1.

We apply strain to our MoS_2 transistors using a two-point bending apparatus, by controlling the distance between the two ends of the substrate, as shown in Figure 2a. The strain can be estimated as $\varepsilon = \tau/(2R)$, where τ = 125 μm is the thickness of the PEN and R is the radius of curvature of the bent substrate (see Figure 2b).[29] The strain applied to the MoS_2 is confirmed by Raman and photoluminescence (PL) spectroscopy, by monitoring the position of the in-plane E′ peak at ∼384 cm^{-1} and the A exciton peak at ∼1.8 eV, respectively. We note that we can only monitor *relative* changes in the MoS_2 strain with bending; i.e., we cannot be sure if the transistor has built-in tensile or compressive strain from the transfer and fabrication process, because the Al_2O_3 gate dielectric can cause peak shifts in the MoS_2 Raman spectra.[30] Thus, all strain measurements below are reported relative to the as-fabricated devices in their flat, unbent state.

Figure 2c shows the Raman spectra of the MoS_2 device from Figure 1b without applied strain (blue) and with ∼0.7% tensile strain (red). We perform Raman measurements on four locations across the device channel with similar results, but only include one representative spectrum at each strain level here for clarity. The E′ peak clearly redshifts with ∼0.7% applied tensile strain, and the average positions of the E′ peaks without and with applied strain are 384.6 ± 0.3 and 383.0 ± 0.2 cm^{-1}, respectively. This corresponds to a peak shift of ∼2.3 ± 0.2 cm^{-1}/% strain, which is comparable to that of other studies.[22,32,33] The cyan curve, representing the measurement after strain is released, matches very well with the initial 0% (blue) curve, indicating that the effects of strain are reversible. Figure S2 of Supporting Information Section 2 includes Raman peak position data for all devices measured and a short discussion of the smaller A_1' peak shifts.

Figure 2d displays the PL spectra of the MoS_2 device from Figure 1b at 0% (blue), 0.4% (magenta), 0.6% (red), and back to 0% strain (cyan). As expected, the A exciton redshifts with tensile strain because of a decrease in the direct, optical band gap at the K point (see Figure 2e).[24,26,34] The A exciton peak positions at 0%, 0.4%, 0.6%, and back to 0% strain are 1.810 ± 0.006, 1.790 ± 0.004, 1.772 ± 0.004, and 1.811 ± 0.005 eV, respectively, averaged over four measurements in the device channel. Therefore, the shift of the A exciton peak is ∼63 ± 10 meV/% strain. This is similar to that of other experimental studies demonstrating the PL of MoS_2 with strain.[24,26,34] The PL peak position data for all devices measured are included in Supporting Information Figure S3b.

Next, we perform electrical measurements of our devices as a function of strain. Our setup enables direct probing of transistors under strain (see Figure 2a) inside a vacuum probe station at ∼2 × 10^{-5} Torr pressure. Figure 3a displays drain current vs gate voltage (I_D-V_{GS}) measurements of the MoS_2 transistor shown in Figure 1b with applied tensile strain from 0% to 0.7%, and back to 0%. The on-state current rises with increasing strain and then returns to the initial (unstrained) level after strain release (cyan curve in Figure 3a). Thus, strain does not have a permanent effect on the device characteristics. The gate leakage currents remain low (<1.2 nA) across all V_{GS} and strain levels (see Supporting Information Figure S4). The drain current vs drain voltage (I_D-V_{DS}) measurements of the device at 0% (solid lines) and 0.7% strain (dotted lines) are displayed in Figure 3b at several V_{GS} values. As before, we observe I_D increasing with strain; for example, at V_{GS} = 7 V and V_{DS} = 5 V, the current doubles from ∼6 μA/μm to ∼12 μA/μm at 0.7% strain.

We estimate the field-effect mobility from the I_D vs V_{GS} curves in the linear operation regime, as $\mu_{FE} = (\partial I_D/\partial V_{GS})L/(WC_{ox}V_{DS})$, where $C_{ox} \approx$ 312 nF/cm^2 is the capacitance per unit area of the gate oxide, extracted from capacitance−voltage measurements of Au−Al_2O_3−Au structures on the same sample as the MoS_2 transistors, with and without strain (see Supporting Information Section 4). We note the threshold voltage (V_T) also changes with strain (see Figure 3a and Supporting Information Figure S11), suggesting that the electron density increases with the decreasing band gap under tensile strain.[33,37] To account for shifts in V_T, we estimate μ_{FE} at the same carrier density $n \sim 1.1 \times 10^{13}$ cm^{-2}, where $n = (C_{ox}/q)(V_{GS} - V_T - V_{DS}/2)$. We estimate V_T with the linear extrapolation method, which uses the voltage intercept of a line fit to the I_D vs V_{GS} near the maximum transconductance $g_m = \partial I_D/\partial V_{GS}$.[38] The transistor has $\mu_{FE} \approx$ 5.3 cm^2 V^{-1} s^{-1} with 0% applied strain and $\mu_{FE} \approx$ 10.8 cm^2 V^{-1} s^{-1} with 0.7% applied tensile strain. Therefore, we achieve a ∼ 2× improvement in μ_{FE} at 0.7% tensile strain for this device, which is essentially the same as the increase in drive current observed in Figure 3b.

We measure 7 other transistors with lengths from L = 2 to 15 μm on the same substrate and perform electrical measurements with applied strain. To account for V_T variation, we extract μ_{FE} at the same carrier density ($n \sim 1.1 \times 10^{13}$ cm^{-2}) and I_D at the same V_{GS} = 7 V and V_{DS} = 1 V, plotting the

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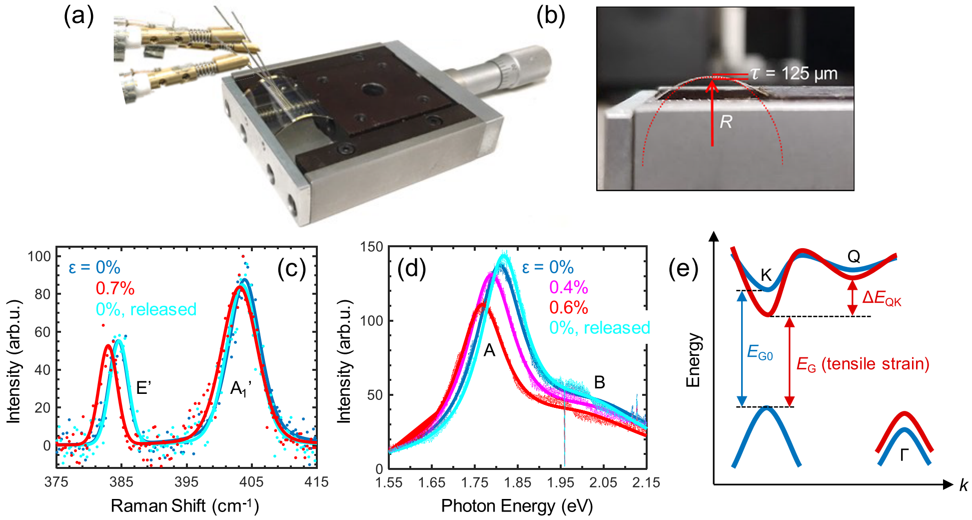

Figure 2. (a) Composite image of bending apparatus for applying tensile strain to the flexible substrates, illustrating the three probes (source, gate, drain) for electrical measurements. (b) Image of bent substrate used to estimate the applied strain $\varepsilon = \tau/(2R)$, where τ is the substrate thickness and R is the radius of curvature. (c) Raman spectra of the device from Figure 1b at different applied strains. The data (symbols) are fit to a superposition of Lorentzian and Gaussian peaks (solid curves). (d) Photoluminescence (PL) spectra of the same device, with the solid line fit to the data as the sum of two Lorentzians, for the A (at ~1.8 eV) and B exciton (at ~2.0 eV).[35,36] The A and B excitons are illustrated in the Figure S3a schematic. The line at ~1.96 eV is due to a Raman notch filter present in the optical path of the measurement setup. All Raman and PL measurements were taken in air, with a 532 nm laser. (e) Simplified band structure of monolayer MoS_2, not to scale. With uniaxial tensile strain, the direct gap at the K point decreases, and the energy separation between K and Q conduction band valleys increases.[12,13,24,26] The valence band at the Γ point also rises, leading to a narrowing of the K−Γ indirect gap[15,26] and the decreased PL intensity observed with strain in Figure 2d.

data for all devices in Figure 3c,d. These show μ_{FE} and I_D normalized to their initial values without applied strain, with the data from all devices summarized by box plots. (Supporting Information Figure S6 shows the magnitudes of μ_{FE} and I_D for each device, without normalizing them.) On average, μ_{FE} increases by a factor of 1.85 ± 0.23, and I_D increases by a factor of 1.76 ± 0.18 with 0.7% applied tensile strain, compared to the initial values without applied strain. For the I_D comparison, we note that the threshold voltage variation is at most $\delta V_T \approx 1$ V, which is significantly smaller than the overdrive voltage $V_{GS} - V_T \approx 8$ V. Therefore, the ~12.5% variation in electron density with δV_T cannot account for the nearly 2× increase in I_D, which must come directly from the tensile strain applied.

Supporting Information Section 5 displays additional strain-dependent data as a function of channel length and at lower carrier density, with results largely consistent with the data presented in Figure 3. We also explored strain levels in excess of 0.7%; however, we generally observed a degradation of electrical device performance in such cases (see Supporting Information Section 6). We attribute this degradation to either worsened adhesion of the contact metal to the MoS_2 or to cracking of the metal lines or Al_2O_3 gate dielectric. "Slippage" of the MoS_2 along the substrate was ruled out because we observed the expected shift of the E′ Raman peak at higher strain levels (Supporting Information Figure S13). In future work, higher strains could be achievable with metals that are more ductile and with gate oxides like HfO_2, which has a lower Young's modulus than Al_2O_3.[39,40]

The improvements in current and mobility of our devices are expected to result from changes in the band structure with strain, as illustrated in Figure 2d,e. The direct band gap of monolayer MoS_2 at the K point decreases with tensile strain, seen as a redshift of the A exciton in Figure 2d. The next-lowest valley in the conduction band is at the Q point (approximately halfway along the T line between the Γ and K points[41−43]), and the energy separation between the Q and K valleys (ΔE_{QK}) has been predicted to increase when tensile strain is applied to MoS_2 (see Figure 2e), resulting in less electron intervalley scattering and therefore improved mobility.[12−14,41] (ΔE_{QK} for monolayer MoS_2 encased in quartz and WS_2 was experimentally estimated to be ~110 meV,[44] and theoretical predictions are in the ~50−270 meV range for unstrained monolayer MoS_2, depending on the simulation approach used.[12−14,41,45,46] Monolayer TMDs such as WS_2, WSe_2, $MoSe_2$, and $MoTe_2$ have smaller ΔE_{QK}; thus, one may expect a larger mobility improvement with strain in transistors based on these materials.[13,46,47])

Tensile strain is also expected to change the curvatures of the conduction band valleys, leading to decreased electron effective mass.[14,15,48,49] This is similar to the reduced electron effective mass with strain in silicon nMOS transistors, which leads to increased mobility.[20,21] Applying tensile strain to 2D transistors has also been suggested to lower Schottky barriers at the source and drain contacts,[33,50,51] potentially leading to lower contact resistance. However, because our devices have relatively long channels and our improvements in μ_{FE} and I_D do not depend on channel length (see Supporting Information Figure S7), we expect the contribution of contact resistance in our measurements to be relatively small.[52] Thus, we believe that the electrical performance improvements observed here are mostly related to electronic transport in the MoS_2 channel, i.e., lower intervalley scattering and effective mass.

We also consider the interaction of strain with defects in our MoS_2 channels. Electron transport in our MoS_2 channels is likely to occur in part by band-like transport, which is limited by scattering with phonons (e.g., intervalley[12,13,41]), defects, or impurities, and in part by hopping-like transport between defect trap states.[53] When strain is applied, the former benefits from lowering of the phonon-assisted intervalley scattering

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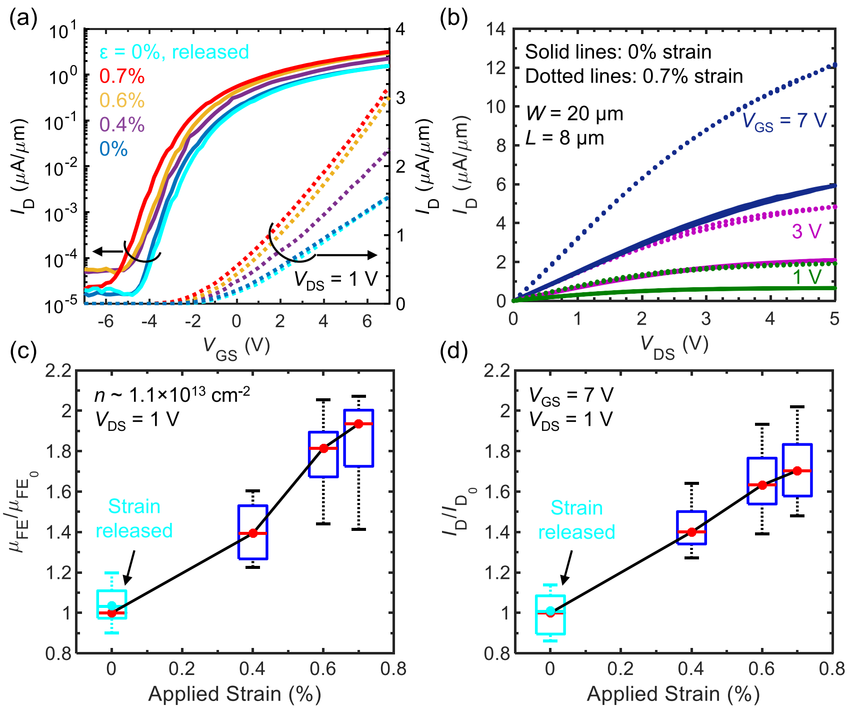

Figure 3. (a) Transfer characteristics (I_D vs V_{GS}) of the device from Figure 1b (W = 20 μm, L = 8 μm) at V_{DS} = 1 V and different levels of applied tensile strain (ε). Solid lines correspond to data plotted on a log scale (left y-axis), and dashed lines represent the same data plotted on a linear scale (right y-axis). (b) Output voltage characteristics (I_D vs V_{DS}) of the same device at 0% (solid) and 0.7% (dotted) applied tensile strain, for V_{GS} = 1 V (green), 3 V (magenta), and 7 V (dark blue). (c) Field-effect mobility (μ_{FE}) normalized to the initial (unstrained) values for 8 devices as a function of applied strain, with box plots showing the median across devices (red points), first and third quartiles (blue box), and maximum and minimum (top and bottom horizontal lines, respectively). The cyan box plot corresponds to the measurement after strain is released. (d) I_D normalized to the initial (unstrained) values at different levels of strain, with box plots again showing the distribution of values across all devices. I_D values were extracted with V_{GS} = 7 V and V_{DS} = 1 V. The cyan box plot again shows the measurement after strain is released.

rate.[12,13,41] On the other hand, tensile strain could also influence the hopping-like transport, as suggested by recent results which saw improvements in carrier lifetime with tensile strain, due to weaker trapping of charge carriers.[54] In other words, tensile strain is expected to benefit the electron mobility for both "pristine", phonon-limited MoS_2 samples, and for lower-quality, "defective" MoS_2 samples.

The large change in resistance with strain of our MoS_2 transistors indicates that these devices could be useful for strain sensors. The figure of merit used to characterize strain sensors is the gauge factor (GF), defined as $(\Delta R/R_0)/\Delta\varepsilon$, where $\Delta R = |R_\varepsilon - R_0|$ is the change in resistance between ε and 0% strain, and R_0 is the initial resistance with 0% applied strain.[55] Metals are often used in commercial strain gauges due to their ease of fabrication, but they typically have relatively low GF < 50.[56] Silicon strain sensors have GF ~ 30−50 for polysilicon[57,58] and up to 200 for single-crystal silicon.[59] 2D materials like MoS_2 and other TMDs are predicted to have large GFs because, similar to silicon and germanium,[60] they are piezoresistive. In addition, they can withstand much higher strains than conventional bulk materials, making them attractive for flexible electronics.[28]

Figure 4a shows the resistance ($R = V_{DS}/I_D$) vs V_{GS} curves for the device in Figure 1b from 0% to 0.7% applied tensile strain. Figure 4b illustrates $\Delta R/R_0$ vs strain for several V_{GS} = −4.4, 0, 3, and 7 V. We find the largest change in resistance at V_{GS} = −4.4 V, which corresponds to the subthreshold region of the transistor (see Figure 3a). Fitting a dashed line to the $\Delta R/R_0$ vs strain at this V_{GS} yields an average GF ≈ 150. Figure 4c shows the calculated GF as a function of V_{GS} for each strain level in Figure 4a. We observe a peak in GF at all strain levels around V_{GS} = −4.4 V, with the maximum GF reaching ~200 for 0.4% tensile strain in this device. (We performed similar measurements on 7 other devices with channel lengths between 2 and 15 μm, and we found an average maximum GF = 200 ± 45.) The GF displays a stronger gate dependence below and near the threshold region (V_{GS} < 0) where current is limited by hopping-like transport between defect trap states,[53] recently shown to more weakly trap carriers when tensile strain is applied.[54] The GF is nearly constant in the linear transistor regime (V_{GS} > 0, also see Figure 3a) where the band-like transport and mobility dominate.

Figure 4d compares the best GF values obtained in this work to those found in the literature for MoS_2, other 2D materials, silicon, and metals (of various thicknesses). Our GF for monolayer CVD-grown MoS_2 is higher than the best GFs for monolayer and trilayer exfoliated MoS_2,[61] CVD-grown MoS_2,[62−64] other 2D materials (BP, InSe, and $PtSe_2$),[65−67] polysilicon,[57,58] and thin metal films.[56] Comparable or slightly higher GFs have been found for bulk crystalline silicon[59,68] and bilayer exfoliated MoS_2,[33,61] respectively. However, CVD-grown MoS_2 is easier to integrate and more promising than bulk silicon or exfoliated MoS_2 for large-area flexible and transparent sensors. We note that Figure 4d only displays GF calculated as $(\Delta R/R_0)/\Delta\varepsilon$, though some studies calculate GF as $(\Delta I/I_0)/\Delta\varepsilon$, where I is current, which artificially yields much larger GF. For example, using the latter definition with current instead of resistance, the maximum GF achieved by our devices would be ~5000 instead of ~200.

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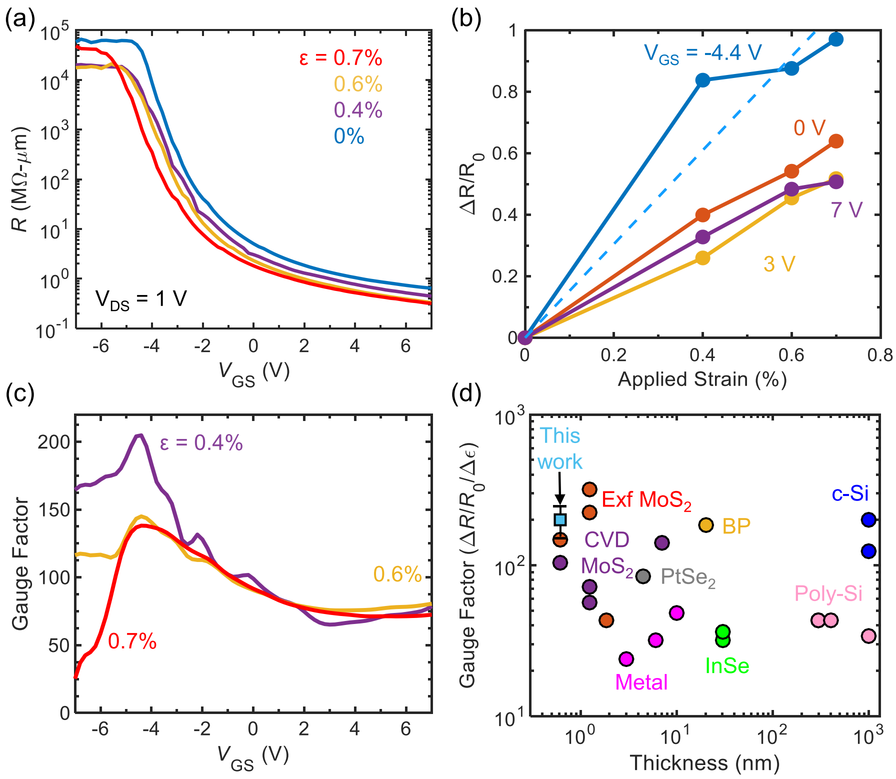

Figure 4. (a) Resistance (R) vs V_{GS} curves of the device in Figure 1b at V_{DS} = 1 V at different levels of applied strain (ε). (b) $\Delta R/R_0$ vs strain at different gate voltages for the curves in panel a. (c) Gauge factor (GF = $(\Delta R/R_0)/\Delta\varepsilon$) vs V_{GS} for the different levels of strain. $\Delta\varepsilon$ is always calculated with respect to 0% strain. The GF below approximately −5 V is uncertain when the measurable I_D minimum is reached (see Figure 3a), suggesting that the peak GF obtained could be higher at lower voltages. (d) GF vs thickness for our best devices (shown as the blue square with error bars) in addition to various materials found in the literature, including CVD-grown MoS_2, exfoliated MoS_2, indium selenide (InSe), platinum selenide ($PtSe_2$), black phosphorus (BP), polycrystalline Si (poly-Si), crystalline Si (c-Si), and thin metal films. We note that the c-Si values are for bulk Si with thicknesses likely greater than 1 μm.

In summary, we studied the mobility enhancement of CVD-grown monolayer MoS_2 transistors with tensile strain, by bending devices on flexible PEN substrates. We found a 2-fold increase of mobility and current with tensile strain up to 0.7%, and a gauge factor (GF) up to ~200, which is the highest reported for sub-1 nm thin piezoresistive films. The improvements are attributed to changes in the band structure, including lower electron−phonon intervalley scattering and lower electron effective mass with tensile strain. These results achieve the largest mobility improvements of MoS_2 transistors with strain to date, pointing the way for performance enhancements in integrated 2D electronics, and for the use of this material in strain sensors on flexible substrates. For electronics on rigid substrates (i.e., integrated with silicon), strain could be induced with nitride or metal layers, or by growth on substrates with different thermal coefficients of expansion or lattice constants.[69−75] Some approaches would have the additional advantage of inducing biaxial strain in the 2D material, which is expected to have a larger effect on the electrical properties than uniaxial strain.[12,23,76,77]

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acs.nanolett.2c01707.

Device fabrication and MoS_2 transfer process, Raman and photoluminescence (PL) spectroscopy of devices with strain, current−voltage characteristics of MoS_2 transistors with strain, $C-V$ characteristics of Au−Al_2O_3−Au capacitors with strain, mobility (μ_{FE}) and drain current (I_D) as a function of strain, and degradation of devices at high levels of strain (PDF)

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Author Contributions

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

Notes

The authors declare no competing financial interest.

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