



High-performance flexible nanoscale transistors based on transition metal dichalcogenides

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Two-dimensional (2D) semiconducting transition metal dichalcogenides could be used to build high-performance flexible electronics. However, flexible field-effect transistors (FETs) based on such materials are typically fabricated with channel lengths on the micrometre scale, not benefitting from the short-channel advantages of 2D materials. Here, we report flexible nanoscale FETs based on 2D semiconductors; these are fabricated by transferring chemical-vapour-deposited transition metal dichalcogenides from rigid growth substrates together with nano-patterned metal contacts, using a polyimide film, which becomes the flexible substrate after release. Transistors based on monolayer molybdenum disulfide (MoS₂) are created with channel lengths down to 60 nm and on-state currents up to 470 $\mu\text{A } \mu\text{m}^{-1}$ at a drain-source voltage of 1 V, which is comparable to the performance of flexible graphene and crystalline silicon FETs. Despite the low thermal conductivity of the flexible substrate, we find that heat spreading through the metal gate and contacts is essential to reach such high current densities. We also show that the approach can be used to create flexible FETs based on molybdenum diselenide (MoSe₂) and tungsten diselenide (WSe₂).

The Internet of Things (IoT) envisions electronics physically present in all aspect of our daily lives—providing information about the machines and environment around us, as well our own bodies. Some of the devices required for this can be created with rigid silicon, but there is also a need for electronics with non-planar form factors^{1,2}, in other words, devices that are thin and light and can be conformally attached to objects with unusual shapes, on human skin or implanted in the body¹. This will require nanoscale flexible electronics that are robust to mechanical strain, easy to integrate, and capable of low-power consumption and high performance^{2,3}.

Two-dimensional (2D) materials are good candidates for flexible electronics due to their lack of dangling bonds, good electron or hole mobility in atomically thin (sub-1-nm) layers, low short-channel effects and ability to be transferred onto different substrates^{2,4-7}. In particular, monolayer transition metal dichalcogenides (TMDs) such as MoS₂ are well-suited for low-power applications due to their electronic band gaps (~ 2 eV)^{8,9}, which enable low off-state currents ($\sim \text{fA } \mu\text{m}^{-1}$)^{10,11}. However, the development of high-performance flexible TMD field-effect transistors (FETs) with nanoscale features is challenging because of difficulties creating such small channel lengths on flexible substrates¹², as well as the fact that the TMD transfer process can lead to contamination or damage of the atomically thin material¹³⁻¹⁵.

The shortest flexible MoS₂ transistors reported so far, which had channel lengths of ~ 68 nm, used three-layer exfoliated material and had on-state currents of $135 \mu\text{A } \mu\text{m}^{-1}$, probably limited by their contact resistance¹⁶. Currently, for large-scale practical applications, MoS₂ must be synthesized by chemical vapour deposition (CVD). The shortest channel length reported for devices based on CVD MoS₂ is ~ 750 nm (with a gate length of ~ 500 nm) with $85 \mu\text{A } \mu\text{m}^{-1}$ on-state current, which is also contact-limited¹⁷. Beyond MoS₂, there have also been some reports on flexible transistors based on other TMDs, such as WSe₂¹⁸⁻²¹. Importantly, achieving a high

transistor on-state current requires both short channels and low contact resistance, for example, by doping the TMD^{22,23} and optimizing the metal-TMD interface^{24,25}.

In this Article, we report flexible monolayer MoS₂ transistors with on-state currents up to $\sim 470 \mu\text{A } \mu\text{m}^{-1}$ at drain-source voltage $V_{\text{DS}} = 1$ V in sub-100-nm channels. The devices are created by transferring the TMDs together with lithographically predefined metal contacts onto flexible substrates. The TMD is grown using CVD on a SiO₂/Si substrate and the critical contact separation is defined while the channel is still on the rigid substrate, enabling the fabrication of nanoscale devices. Flexible polyimide (PI) is spin-coated onto the pre-patterned structures and they are released together, with the remaining process continuing on the PI. The approach is also used to create flexible FETs based on MoS₂, WSe₂ and MoSe₂, all of which have staggered device configurations²⁶; that is, the channel is sandwiched between the source/drain and the gate.

Transfer process with embedded contacts

The TMDs were grown by CVD on SiO₂/Si substrates as previously reported²⁷⁻³⁰. Information on substrate preparation and MoS₂ properties, including Raman, photoluminescence (PL), atomic-force microscopy and layer homogeneity, is provided in Supplementary Sections 1 and 2, and details about the Au liftoff process are given in the Methods. Subsequently, we lithographically patterned Au metal contacts on top. We chose Au without an adhesion layer because of its good contact resistance²⁴ (R_c) to MoS₂ and its low adhesion to SiO₂³¹. Both the Au and TMD (lacking out-of-plane dangling bonds) can be released from the SiO₂ surfaces without damage, as shown below. After the contacts were defined, we conformally covered the pre-patterned structures with $\sim 5 \mu\text{m}$ of PI, which was released, together with the TMD and Au, from the SiO₂/Si growth substrate by immersion and agitation in deionized (DI) water (Methods). Although performing the entire device fabrication before transfer could be envisaged, most dielectrics will stick to the SiO₂ substrate

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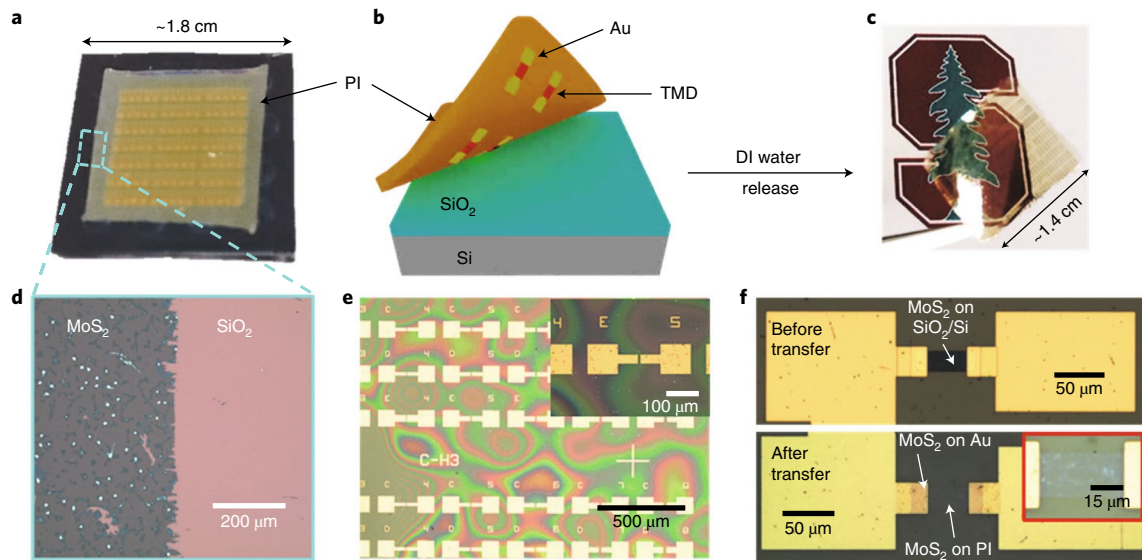


Fig. 1 | Transfer process for 2D monolayers with contacts. **a**, Optical image of MoS₂ and patterned metal, covered by PI, on SiO₂/Si. **b**, Schematic of the transfer process. The PI with embedded metal contacts and monolayer TMD are released from the rigid growth substrate. **c**, Optical image of the flexible PI after transfer. **d–f**, Optical microscope images of the SiO₂/Si growth substrate left behind after transfer (with the bare SiO₂ surface where MoS₂ had been previously covered by PI) (**d**), the PI film with contacts and unpatterned MoS₂ after transfer (**e**) and contacts with patterned MoS₂ on SiO₂/Si (**f**, top) and PI (**f**, bottom). Insets show close-ups of FET channels. Raman and PL spectra of MoS₂, WSe₂ and MoSe₂ before and after transfer are shown in Supplementary Section 4.

and complicate the release procedure. Thus, we decided to continue processing the gate stack after transfer to the PI substrate (as further described below and in the Methods).

Figure 1a shows the SiO₂/Si substrate with TMD, contacts and PI, Fig. 1b displays the release schematic and Fig. 1c shows the transparent PI substrate after release. We note that a similar damage-free transfer of MoS₂ layers (without contacts) for coplanar²⁶ micrometre-sized FETs has recently been demonstrated over 4-inch wafers³², indicating that this approach could be scaled up. The optical image in Fig. 1d shows that the TMD (here MoS₂) is completely delaminated from the area that had been covered by PI on the SiO₂/Si substrate. Note that agitation in DI water also causes some delamination of MoS₂ in the area that is not covered by PI (for example, at the bottom left and edges). We can transfer continuous (Fig. 1e) as well as pre-patterned (Fig. 1f) MoS₂ films with embedded contacts, enabling us to realize devices based on a number of fabrication approaches. As shown later, we have fabricated FETs with MoS₂, MoSe₂ and WSe₂, where only the contacts were patterned before transfer, minimizing the process steps on unprotected TMDs (Fig. 1e and Supplementary Section 3), but leading to channel widths greater than the electrode widths (referred to as type A devices). We also realized FETs where the MoS₂ channel was pre-defined by reactive ion etching (RIE) before transfer (Fig. 1f), which enables accurate channel width definition (referred to as type B). Further details on device fabrication are provided in the Methods.

To confirm that the TMDs remain intact throughout the transfer process, we performed extensive Raman spectroscopy and PL measurements before and after transfer (Supplementary Section 4). We observe that the PI background signal and quenching on Au surfaces^{33,34} affect the resolution and visibility of TMD peaks. The Raman and PL spectra on SiO₂/Si indicate TMDs with monolayer thickness; however, MoSe₂ also had regions with bilayers (Supplementary Section 4). Generally, the absence of major changes in the Raman and PL results before and after transfer indicates that mono- as well as multilayer TMDs can be readily transferred with this technique, without apparent damage. In addition, we found that the surface roughness does not discernibly increase after transfer, preserving

root-mean-square roughness below 0.5 nm (Supplementary Section 2). The electrical results presented in the following further confirm the excellent viability of this transfer approach.

Flexible top-gated FETs

After the transfer process, the material stack was flipped with the source and drain contacts embedded in the PI substrate and the TMD semiconductor on top. To prevent contamination of this exposed TMD surface, we deposited an Al₂O₃ gate dielectric immediately after the transfer process and before any other patterning steps. The fabrication process was finalized with gate metal definition, leading to a staggered device geometry. For MoS₂ FETs of type A, we used RIE to pattern the channel and gate dielectric together, after gate metal deposition, but channels of type B devices were already patterned by RIE before transfer (additional fabrication details are provided in the Methods). The device cross-section is schematically shown in Fig. 2a, and Fig. 2b–d displays optical images of the WSe₂, MoSe₂ and MoS₂ FETs. Measured transfer and output characteristics of micrometre-scale FETs with WSe₂, MoSe₂ (both type A) and MoS₂ (type B) are presented in Fig. 2e–j, respectively. All display n-type behaviour, because electron conduction is typically dominant for evaporated Au contacts to these materials^{20,35}.

The extracted device parameters for all TMDs are listed in Table 1. Threshold voltage (V_T) and extrinsic field-effect mobility ($\mu_{FE,ext}$) were estimated at the maximum transconductance (g_m), using the measured Al₂O₃ gate oxide capacitance ($C_{ox} = 0.21–0.32 \mu\text{F cm}^{-2}$) from the TMD FETs obtained in accumulation (Supplementary Section 5)³⁶. The $\sim 1.7\text{-}\mu\text{m}$ -long monolayer WSe₂ FET exhibits a maximum on-state current of $I_D = 3.6 \pm 0.1 \mu\text{A } \mu\text{m}^{-1}$ (the source of the error bars is explained below) at a drain–source voltage of $V_{DS} = 1\text{ V}$, which is over twice larger than the highest previously reported for flexible WSe₂ (using bilayer exfoliated material)¹⁸. The $\sim 2.7\text{-}\mu\text{m}$ -long MoSe₂ FET reaches $I_D = 4.2 \pm 0.4 \mu\text{A } \mu\text{m}^{-1}$ at $V_{DS} = 4\text{ V}$, which is also a clear demonstration of flexible MoSe₂ FETs.

The mobility and width-normalized current of type A devices are listed with error bars because their channel width was not patterned and they were subject to (some) current spreading effects,

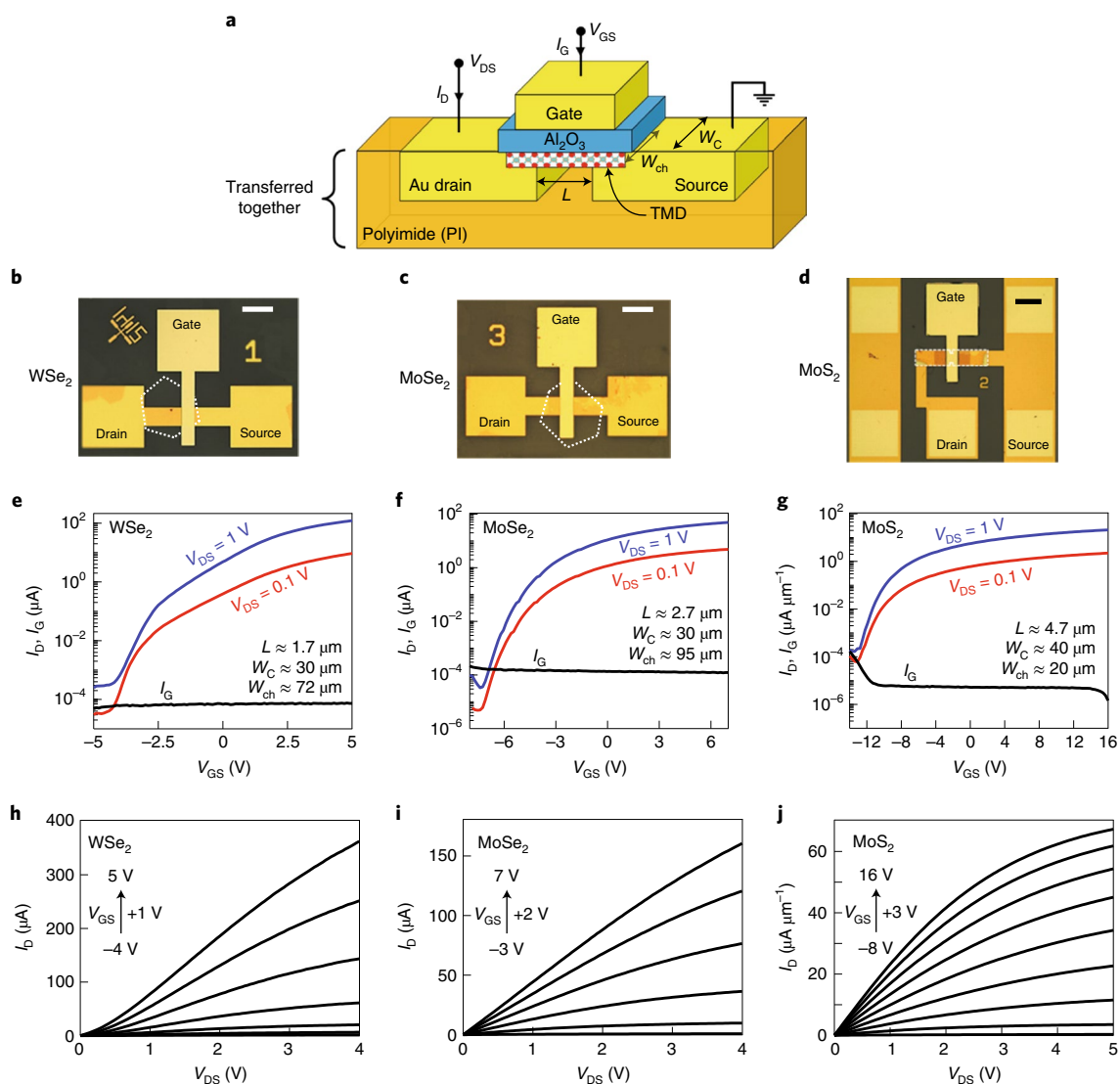


Fig. 2 | Flexible FETs with TMDs. **a**, Schematic cross-section. **b–d**, Optical microscope images of FETs with WSe₂ (type A) (**b**), MoSe₂ (type A) (**c**) and MoS₂ (type B) (**d**). The white dotted lines mark the outline of the 2D materials. Scale bars, 50 μm . **e–j**, Measured transfer and output characteristics of WSe₂ (type A) (**e,h**), MoSe₂ (type A) (**f,i**) and MoS₂ (type B) (**g,j**). Red and blue lines in **e–g** represent drain current, I_D . The gate current (I_G) is often negligible, although for some devices it can limit the on/off ratio.

which we account for with numerical simulations (Supplementary Section 15). For example, the unpatterned hexagonal crystals for the Se-based FETs are shown in Fig. 2b,c. Their measured data are shown in plain current units (μA) in Fig. 2e,f and Fig. 2h,i, respectively, but the error bars are included when presenting their width-normalized current ($\mu\text{A } \mu\text{m}^{-1}$), for example in Table 1.

The correction is not needed for our type B devices because of the optimized geometry and modified fabrication process. Hence, Fig. 2g,j, for type B MoS₂ FETs, is displayed in width-normalized units and the better quality of this material also enables larger $I_D \approx 67.3 \mu\text{A } \mu\text{m}^{-1}$ in a $\sim 4.7\text{-}\mu\text{m}$ -long FET at $V_{DS} = 5\text{ V}$. In comparison, type A MoS₂ FETs had higher subthreshold swing (SS) and off-state current, reducing their on/off ratio (Table 1 and Supplementary Section 6). Furthermore, the process flow for type B devices facilitates the fabrication of circuits, and an example inverter is shown in Supplementary Section 7. Comparing device hysteresis³⁷, we find it ranges from $\sim 0.1\text{ V}$ (WSe₂) to $\sim 1.6\text{ V}$ (MoSe₂) for all devices and TMDs, indicating that the additional patterning step of type B devices does not deteriorate TMD interfaces

(Supplementary Section 8). We have also verified the stability of the flexible TMD FETs under tensile bending and found no notable changes for a bending radius of 4 mm or a tensile strain of $\sim 0.063\%$ (Supplementary Section 9).

Nanoscale flexible MoS₂ transistors

As MoS₂ has the most mature growth process with the highest electrical quality and best surface coverage, we further studied its FET scaling down to $\sim 60\text{ nm}$ (Supplementary Section 10) with electron-beam lithography (EBL) for source–drain contact patterning. Importantly, this nanoscale resolution is enabled by our approach, wherein the contact patterning is first performed on the atomically smooth SiO₂/Si surface instead of the PI, which is prone to waviness, enhanced charging effects and possible damage in EBL³⁸. We also verified that this process is benign to MoS₂, performing Raman and PL measurements before and after EBL, finding no apparent evidence of damage to the MoS₂ (Supplementary Section 11). The remaining device fabrication and transfer were performed as described above.

Table 1 | Electrical parameters of flexible FETs

Device	Channel length (nm)	$\mu_{FE,ext}$ ($\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$)	I_D at $V_{DS} = 1 \text{V}$ ($\mu\text{A} \mu\text{m}^{-1}$)	V_T (V)	SS (mV dec $^{-1}$)	On/off ratio
WSe $_2$ (type A)	1,700	4.1 ± 0.1^a	3.6 ± 0.1^a	1.6	380	3×10^5
MoSe $_2$ (type A)	2,700	1.2 ± 0.1^a	1.3 ± 0.1^a	-2	430	1×10^6
MoS $_2$ (type A)	4,700	14.2 ± 2.2^a	5.5 ± 0.9^a	3.9	1,700	3.6×10^3
MoS $_2$ (type B)	4,700	24	21	-5.2	850	1×10^5
MoS $_2$ (type B)	112	8.1	229	0.6	730	2×10^6
MoS $_2$ (type A)	82	23.2 ± 1.4^a	466 ± 40^a	6	1,000	4×10^3

The extrinsic field-effect mobility $\mu_{FE,ext}$ and threshold voltage V_T were extracted from the maximum g_m in the linear operating regime at a drain-source voltage $V_{DS} = 0.1 \text{V}$. The subthreshold swing (SS) value denotes the extracted minimum. We note some V_T variability, which is not unusual for 2D transistors in academic fabrication facilities. ^aValues corrected for current spreading.

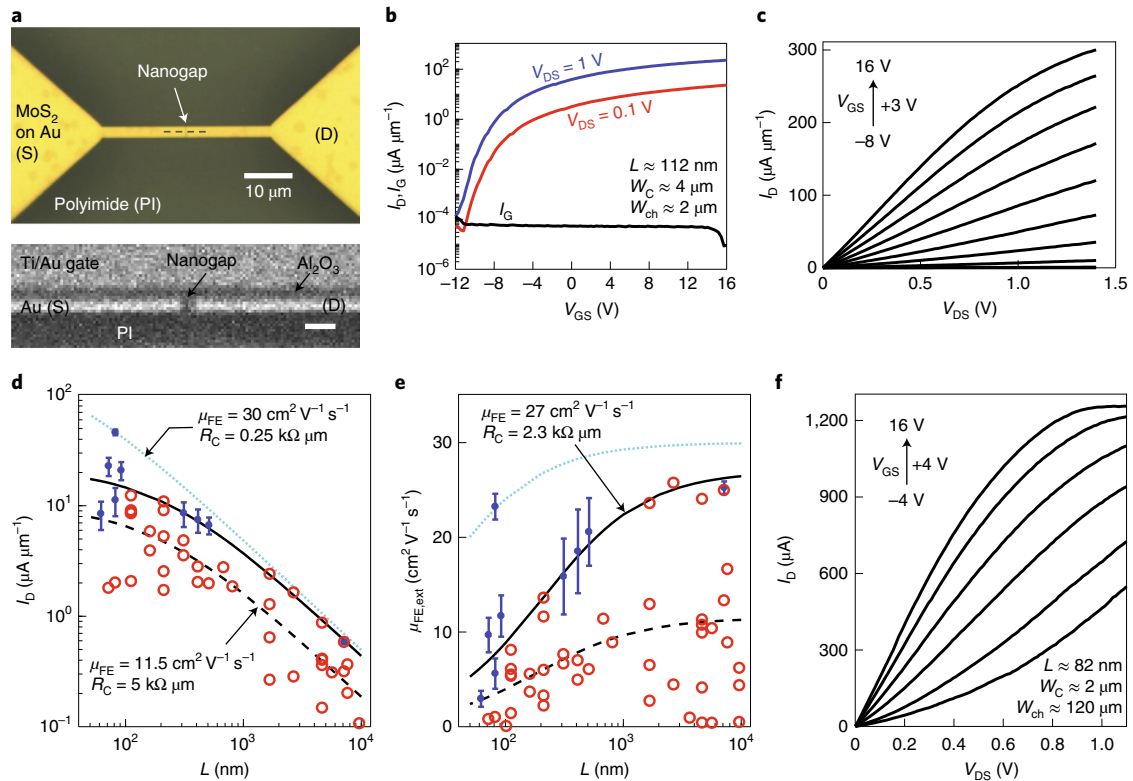


Fig. 3 | Nanoscale MoS $_2$ FETs. **a**, Optical microscope image of a nanoscale channel after transfer (top) and cross-section scanning electron microscopy (SEM) image of a transistor with channel length (L) of ~ 100 nm (bottom; scale bar, 200 nm). The cross-section is taken along the dashed line in the top image. **b, c**, Transfer (**b**) and output (**c**) characteristics of a type B MoS $_2$ FET with $L \approx 112$ nm. **d, e**, Drain current I_D (**d**) and extrinsic field-effect mobility $\mu_{FE,ext}$ (**e**) as a function of L for ~ 50 devices at a drain-source voltage of $V_{DS} = 0.1 \text{V}$ and an overdrive voltage of $V_{GS} - V_T = 8 \text{V}$. Solid black and dashed black lines illustrate a fitted trend for ‘best’ and ‘typical’ type B devices (red circles), while the blue dotted lines include the best type A device (blue symbols). Error bars of blue symbols represent uncertainty due to corrections for current spreading. **f**, Electrical characteristics of a MoS $_2$ FET (type A) with $L \approx 82$ nm, showing remarkably high $I_D > 1.2 \text{mA}$, which is $\sim 470 \mu\text{A} \mu\text{m}^{-1}$ after current spreading correction.

Figure 3a presents a top-view optical image of a nanoscale channel after transfer and a post-fabrication-device cross-section. The cross-section shows that the Al $_2$ O $_3$ gate dielectric covers the planar source and drain electrodes, including the ~ 100 -nm nanogap between them, illustrating the absence of ‘steps’ in the surface topography enabled by this fabrication technique with contacts embedded in the flexible substrate (Supplementary Section 2). Electrical measurements of a similar type B device with ~ 112 -nm-long channel are shown in Fig. 3b,c, showing a good on/off ratio ($> 10^6$), high $I_D \approx 303 \mu\text{A} \mu\text{m}^{-1}$ (at $V_{DS} = 1.4 \text{V}$) and $\mu_{FE,ext} \approx 8.1 \text{cm}^2 \text{V}^{-1} \text{s}^{-1}$. The mobility appears smaller than in micrometre-scale devices due to the greater contribution from R_C , as discussed in the following (for other device parameters see Table 1).

The measured output characteristics (Fig. 3c,f) show signs of self-heating and velocity saturation^{23,39} due to the onset of current saturation at lower V_{DS} with higher gate-source voltages V_{GS} , which is similar to the self-heating of MoS $_2$ FETs on SiO $_2$ /Si substrates. We estimate that the temperature of this FET channel exceeds 350 °C at the peak input power in Fig. 3f, but the PI remains below its glass transition temperature because the device heat spreading occurs primarily through the gate stack and contacts (Supplementary Section 12). To gain additional insight into intrinsic device parameters, we extracted I_D (at an overdrive $V_{ov} = V_{GS} - V_T = 8 \text{V}$) and $\mu_{FE,ext}$ for channel lengths from ~ 60 nm to $\sim 10 \mu\text{m}$ in Fig. 3d,e. Measuring numerous devices allows us to comment both on ‘typical’ and ‘best-case’ device performance. We used a model that relates I_D and $\mu_{FE,ext}$ to L ,

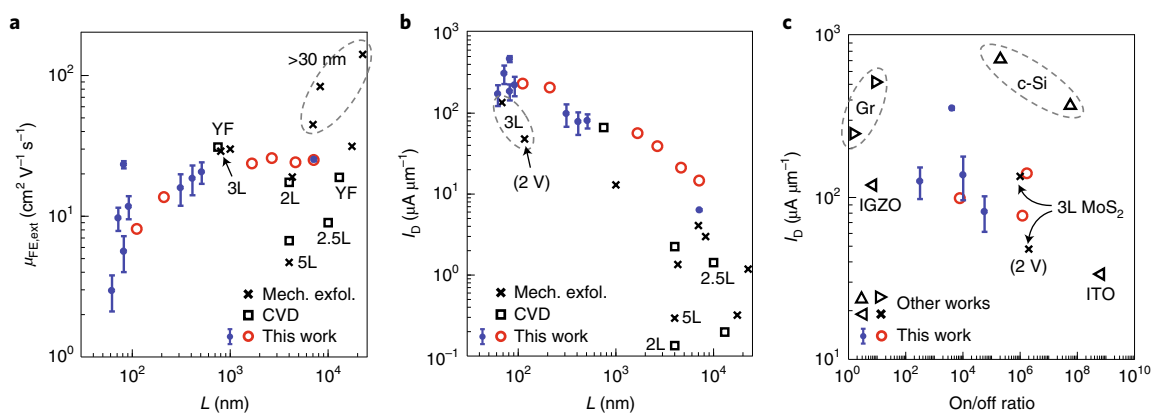


Fig. 4 | Benchmarking flexible FETs. **a, b**, Extrinsic field-effect mobility $\mu_{FE,ext}$ (**a**) and drain current I_D (at $V_{DS}=1$ V) (**b**) for flexible MoS₂ transistors as a function of channel length (L)^{4,16,17,32,44–53}. Three studies reported μ_{FE} excluding contact resistance, with the y-function method (YF). A few points correspond to three-layer (3L) MoS₂, one of them at $V_{DS}=2$ V, one ($L=68$ nm) at unspecified voltage. Most CVD-grown MoS₂ are monolayers (1L); the other thicknesses are as labelled up to five layers (5L), and unlabelled points are all thicker exfoliated channels. All thicknesses and more details from other works are listed in Supplementary Section 16. The MoS₂ films in this work are mostly monolayers with some multilayer islands (up to 34%; Supplementary Section 1). **c**, Reported I_D (at $V_{DS}=0.5$ V) versus on/off current ratio for flexible FETs with channel $L \leq 200$ nm (refs.^{43,54–58}). For comparison, two data points are shown for graphene (Gr), two for crystalline silicon (c-Si), two for oxide semiconductors (indium tin oxide (ITO) and indium gallium zinc oxide (IGZO)) and the others for MoS₂ (our CVD monolayer data and two reports on 3L exfoliated). Blue and red symbols are type A and B devices from this work, respectively. Error bars on blue symbols represent uncertainty from current spreading correction.

R_C and the intrinsic field-effect mobility μ_{FE} . (The adapted model⁴⁰, the V_T and $\mu_{FE,ext}$ extractions are described in Supplementary Sections 5 and 14.) Figure 3d,e shows that I_D plateaus and $\mu_{FE,ext}$ decreases at sub-1-μm channel lengths, which clearly indicates that these devices are limited by R_C . The dashed black lines show the model for ‘typical’ type B devices (red circles), which we fitted with an average μ_{FE} (~ 11.5 cm² V⁻¹ s⁻¹) for micrometre-scale devices where the impact of R_C is small, and by setting $R_C=5$ kΩ μm to follow the middle of the distribution for shorter L .

The solid black lines in Fig. 3d,e are based on a similar approach but using higher μ_{FE} (~ 27 cm² V⁻¹ s⁻¹) to fit the best-performing type B devices with $R_C=2.3$ kΩ μm. Also taking into account the ‘best’ type A devices (blue symbols and error bars, corrected for current spreading), we fit $R_C \approx 250$ Ω μm for one device (at $L \approx 82$ nm) and a slightly higher $\mu_{FE}=30$ cm² V⁻¹ s⁻¹, generating the blue dotted lines. The FET with highest on-state current achieves an impressive $I_D=466 \pm 40$ μA μm⁻¹ at $V_{DS}=1$ V (Supplementary Section 13 provides electrical data and Supplementary Section 15 the current spreading correction), and its electrical characteristics are shown in Fig. 3f and Supplementary Fig. 22b. The presence of a ‘hero’ device is not surprising when dozens (or hundreds²⁸) of devices are measured, being both an indicator of academic fabrication and growth variability, and of the promise of these 2D semiconductors if variability challenges are eventually mitigated by industrial optimization. (We note that our type A and B devices have similar variability; Supplementary Section 13.)

Our estimated best-case μ_{FE} and R_C are comparable to the best reported values for monolayer MoS₂ on flexible substrates and on SiO₂/Si rigid substrates, respectively^{17,28,39}. The highest on-state current, I_D , is over three times greater than in previous reports for flexible MoS₂ FETs¹⁶, similar to the best TMD FETs on rigid substrates⁴¹, and even comparable to flexible FETs based on graphene⁴² and crystalline Si (c-Si)⁴³. Moreover, this fabrication technique enables us to scale flexible MoS₂ FETs to the shortest channel lengths reported so far (Supplementary Fig. 22c).

Figure 4 displays benchmarking of our flexible MoS₂ transistors compared to other technologies on flexible substrates. Displaying the extrinsic mobility $\mu_{FE,ext}$ and drain current I_D (at $V_{DS}=1$ V, unless noted otherwise) for flexible MoS₂ FETs versus L (Fig. 4a,b) reveals that nanoscale devices have received little attention until now (values are listed in Supplementary Table 2)^{4,16,17,32,44–53}. Figure 4c compares

the on-state current and on/off ratio of the few existing sub-200-nm flexible FETs (at $V_{DS}=0.5$ V, unless noted otherwise), showing the good performance of our MoS₂, even next to high-mobility materials (values are listed in Supplementary Table 3)^{43,54–58}. The on/off ratio of MoS₂ is many orders of magnitude higher than graphene (on/off <10), making MoS₂ more suitable for low-power applications among existing 2D channel materials. Compared to flexible c-Si FETs, flexible TMD FETs have a fundamentally different structure, with a sub-nanometre thin channel without out-of-plane dangling bonds. This enables shorter channel lengths, better mechanical robustness and potentially lower cost (due to the simple transfer processes), all of which are advantageous for higher-performance and lower-power operation on flexible substrates.

Conclusions

We have reported high-performance MoS₂ transistors on flexible substrates, created using a transfer process that includes nano-patterned contacts. The approach allows devices with channel lengths as low as ~ 60 nm to be fabricated. Our devices exhibit drive currents up to ~ 470 μA μm⁻¹ at $V_{DS}=1$ V, among the highest for any monolayer 2D semiconductor, including those on rigid Si substrates. The on-state current is also comparable to those of flexible graphene and c-Si transistors, while maintaining an on/off current ratio over 10⁴. The high current is achieved despite the low thermal conductivity of the PI substrate, as the short channel devices benefit from heat spreading through the gate and contacts. We have also shown that the fabrication technique can be applied to other 2D semiconductors, creating flexible MoSe₂ and monolayer WSe₂ FETs. Our approach could be used as a template for making flexible transistors with other materials that have few demonstrations of short-channel devices, including oxides, organics and carbon nanotubes. Together with further optimization of electrostatic control (such as thinner gate dielectrics or double gates) and reduced parasitics (such as lower parasitic capacitance; Supplementary Section 17), the technique could allow flexible TMD electronics to be incorporated into low-power and high-performance IoT applications.

Methods

Raman and PL measurements. The Raman and PL measurements were performed on a HORIBA Scientific LabRAM HR Evolution spectrometer using an excitation

wavelength of 532 nm. For the Raman measurements on SiO₂/Si, for acquisition time, accumulations, laser power and optical grating we used 5 s, 3, 0.14 mW and 1,800 gr mm⁻¹, and the spot size was less than 1 μm. For the Raman measurements after transfer on PI or Au/PI surfaces, the acquisition time was increased to 45 s, while the other parameters remained the same. For PL measurements on SiO₂/Si, PI and Au/PI, the acquisition time, accumulations, laser power and optical grating were 5 s, 3, 0.14 mW, 600 gr mm⁻¹.

Device fabrication including transfer process and liftoff procedure. *Fabrication of type A devices, channel defined last.* The TMDs were grown on Si/SiO₂ substrates with CVD, as previously reported^{27–30}. For device fabrication, 45-nm-thick Au source and drain contacts were first deposited by electron-beam evaporation and patterned by liftoff. Optionally, the adhesion of metal contacts to the subsequently spin-coated PI could be improved by evaporating an additional Ti layer on top of the Au before liftoff, but we have not observed discernible differences in transfer efficacy by doing so. The lithographic patterning for that step was carried out using optical lithography (Heidelberg MLA 150 direct write lithography tool) for micrometre-scale channel lengths, and via EBL for sub-micrometre-scale channel lengths (parameters are listed in the following). Then, ~5-μm-thick PI (PI-2610, HD Microsystems) was spin-coated on top, baked at 90 °C and 150 °C on a hot plate, each for 90 s, and finally cured in a nitrogen oven at 250 °C for 30 min. Before PI spin-coating, the outside edges of the silicon substrate were protected with tape to facilitate the release of PI from the Si substrate (Fig. 1a). The transfer was performed in DI water by initially mechanically releasing the outside edges with a tweezer followed by agitation until the PI substrate (with the metal contacts and TMD) floated on the DI water surface. After nitrogen blow-drying the substrate, a 1.5-nm-thick Al blanket film was deposited on top by electron-beam evaporation. This film acts as a seed layer for the subsequent atomic-layer deposition of an Al₂O₃ gate dielectric at 200 °C. Note that we used 35-nm Al₂O₃ for the MoS₂ devices and 23-nm-thick Al₂O₃ for the MoSe₂ and WSe₂ devices. This yields C_{ox} ≈ 0.21–0.32 μF cm⁻², as directly measured in Supplementary Fig. 12. The oxide thicknesses were chosen to ensure higher device yield and to have numerous FETs for measurement. After the atomic-layer deposition, the gate metal was deposited by electron-beam evaporation of Ti/Au (5/60 nm) and patterned by optical lithography and liftoff. This concluded the fabrication for MoSe₂ and WSe₂ devices. For MoS₂ devices, as a final step, the Al₂O₃ and MoS₂ were patterned together using RIE (Oxford 80 RIE) in CF₄/O₂ at gas flows of 50 s.c.c.m.:5 s.c.c.m., power of 150 W and a pressure of 30 mtorr.

Fabrication of type B devices, channel defined before transfer. Up to the source and drain contact metallization, the fabrication of the type B device is the same as for the type A device. However, after source and drain metallization, the MoS₂ channels were patterned by RIE (Oxford 80 RIE) in CF₄/O₂ at gas flows of 50 s.c.c.m.:10 s.c.c.m., power of 100 W and pressure of 30 mtorr, followed by surface cleaning with O₂ plasma (20 W, 10 mtorr, 40 s.c.c.m.) in the same tool. Then, contact pads and leads were defined by optical lithography, electron-beam evaporation of Au/Ti (60 nm/5 nm) and liftoff (a Ti layer on top of Au is optional, as discussed for the type A fabrication). This was followed by PI spin-coating, curing and transfer of all structures in the same way as described for the type A devices. After gate dielectric deposition (same as for the type A devices), via holes for probing, source and drain electrodes were wet-etched in Al etchant at 40 °C. Finally, the gate metallization was performed similarly as for the type A devices.

Liftoff procedure. The source and drain contacts in this work consist of bare Au, which is known to have poor adhesion, especially to SiO₂³¹. Thus, we needed to perform this step carefully to avoid delamination of the electrodes. The procedure is the same for liftoff after optical lithography and after EBL. In both cases, we used a double layer of resist (LOL2000 and SPR3612 from Shipley for optical lithography; see next section for EBL), which provided an undercut in the resist stack. Thus, the Au, which was evaporated on top of the entire sample, is disconnected over the resist steps. This is important, because we wish to avoid strong mechanical forces (for example, no sonication), which could delaminate either the Au or the TMD. After the Au was evaporated on top of the resist stack, we soaked the samples for >12 h in N-methyl pyrrolidone (for optical lithography) or acetone (for EBL). The Au was then gently removed from undesired locations by pulsing the solvent over the sample surface with a pipette. This step lifted off most metal (>95% by visual inspection), but to remove remaining stubborn metal residue, the samples were immersed in acetone followed by isopropanol, and gentle solvent pulsing with a pipette was applied in each solvent. Finally, the samples were removed from the isopropanol and nitrogen blow-dried.

EBL on MoS₂. We used a double layer of poly(methyl methacrylate) (PMMA) for liftoff patterns defined by EBL. The bottom and top layer were 50-nm-thick 495 K A2 PMMA and 200-nm-thick 950 K A4 PMMA, respectively. EBL was performed on a JEOL JBX 6300 lithography system at a dose of 900 μC cm⁻² and an acceleration voltage of 100 kV.

Electrical measurements. All transistors were tested with a Keithley 4200 system on a probe station in ambient air. For the bending experiments, the substrates were attached to a metallic cylindrical rod with a radius of 4 mm.

Data availability

The data that support the plots within this paper and other findings of the study are available from the corresponding author upon reasonable request.

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Author contributions

A.D. conceived the work and performed the device fabrication and characterization. A.D. and S.V. developed the TMD transfer process. R.W.G. performed the MoS₂ CVD growth and C.S.B. the WSe₂ and MoSe₂ CVD growths. V.C. carried out the electron beam lithography and atomic-force microscopy. A.D. and K.S. performed optical material analysis with help from K.B. H.R.L. carried out scanning electron microscopy. C.K. set up numerical current spreading simulations and thermal simulations with E.P. A.D. analysed all data and wrote the manuscript with help from V.C., C.K. and E.P. All authors revised and commented on the manuscript. E.P. supervised the work.

Competing interests

The authors declare no competing interests.

Additional information

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Supplementary information

High-performance flexible nanoscale transistors based on transition metal dichalcogenides

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Supplementary Information

High-performance flexible nanoscale transistors based on transition metal dichalcogenides

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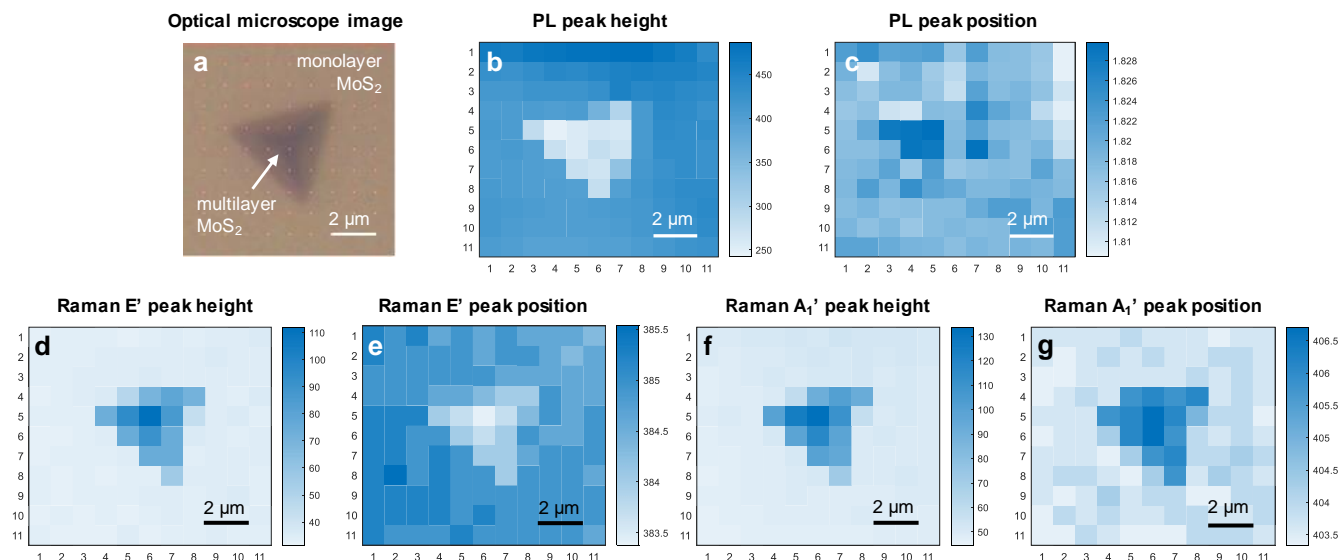
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1. MoS₂ film properties, growth conditions, SiO₂/Si substrate preparation

MoS₂ was synthesized by CVD growth as described in prior work.^{27,28} The SiO₂/Si substrates were pretreated by hexamethyldisilazane (HMDS) vapor to provide a hydrophobic surface for the subsequently applied seeding promoter (PTAS, i.e. perylene-3,4,9,10 tetracarboxylic acid tetrapotassium salt dissolved in DI water and dried on a hot plate) on the edges of the chip, which prevents spreading towards the chip center. The same substrate treatments were applied for the growth of the other TMDs. The MoS₂ growth from solid precursors (MoO₃ and S) then forms large single crystal triangles with sizes in the order of tens of microns which coalesce into a continuous film in the chip center, and non-continuous areas closer to the chip edge (see Fig. 1 in previous work²⁷).

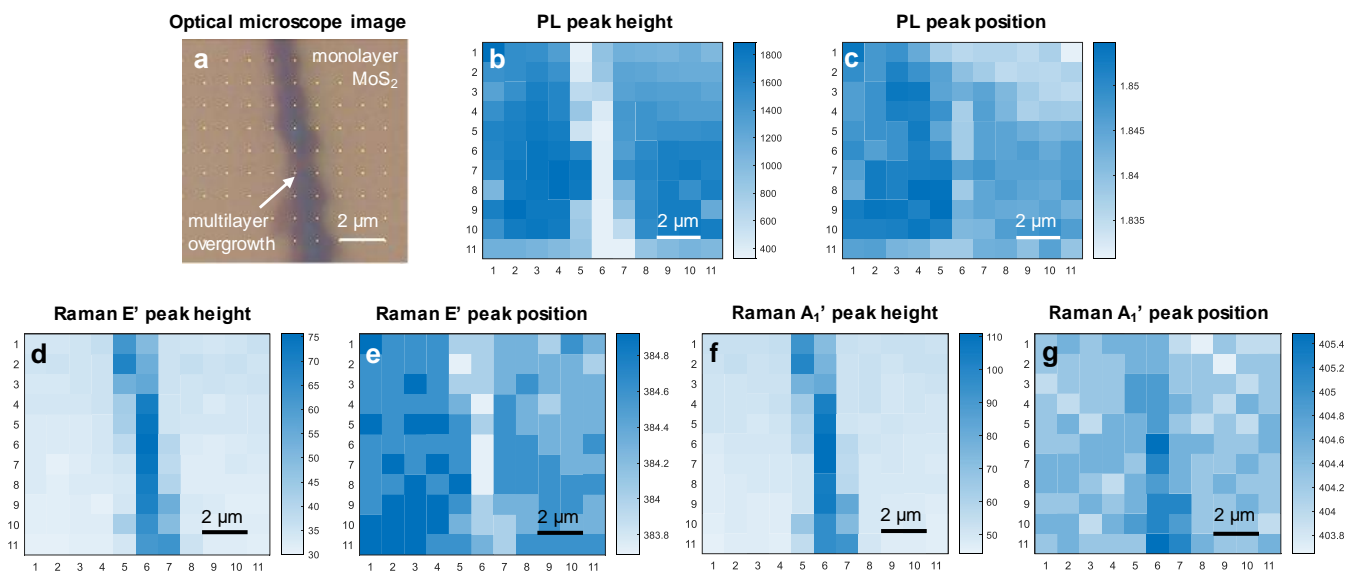
Although the MoS₂ film can essentially be characterized as a monolayer film, some small multilayer islands and overgrowth are present at grain boundaries or nucleation sites. Supplementary Fig. 1 and 2 display Raman and photoluminescence (PL) mapping of a multilayer region and grain boundary, respectively, each surrounded by monolayer MoS₂. As visible from the peak positions, the Raman peak separation is increased in these multilayer regions suggesting a thickness of about 2-3 MoS₂ layers.⁵⁹

The amount of overgrowth and multilayers can vary depending on the location on the sample (edge vs. center) and between growths. This is further quantified by optical image analysis performed on samples used for flexible devices based on the transfer process described in this work. Supplementary Fig. 3a,b shows examples where unpatterned MoS₂ was transferred together with contacts (for *Type A* devices)

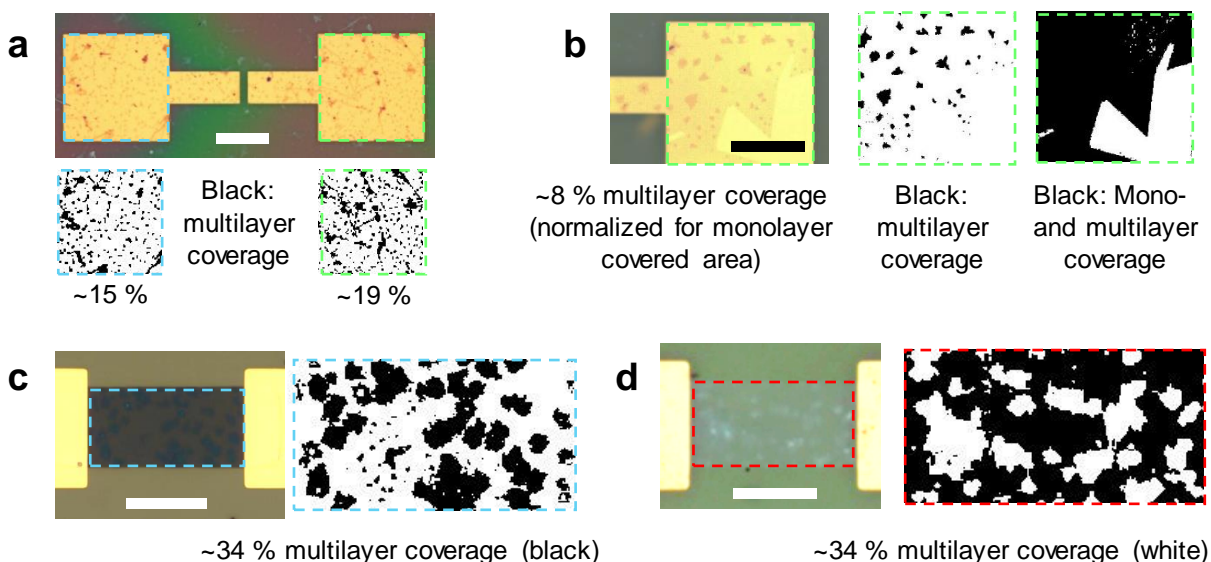


Supplementary Fig. 1 | Raman and photoluminescence (PL) mapping of an MoS₂ multilayer island surrounded by monolayer MoS₂ on SiO₂/Si. a, Optical image of mapped area. b, PL peak height. c, PL peak position. d, Raman E' peak height. e, Raman E' peak position. f, Raman A₁' peak height. g, Raman A₁' peak position.

from the center of the chip (a) and from the chip edge (b). The threshold brightness analysis of these images indicates a multilayer coverage of 8-19%. For another example of *Type B* devices during processing (located in chip center), we find that the multilayer coverage can be as high as 34 %



Supplementary Fig. 2 | Raman and photoluminescence (PL) mapping of an MoS₂ grain boundary surrounded by monolayer MoS₂ on SiO₂/Si. a, Optical image of mapped area. b, PL peak height. c, PL peak position. d, Raman E' peak height. e, Raman E' peak position. f, Raman A₁' peak height. g, Raman A₁' peak position.

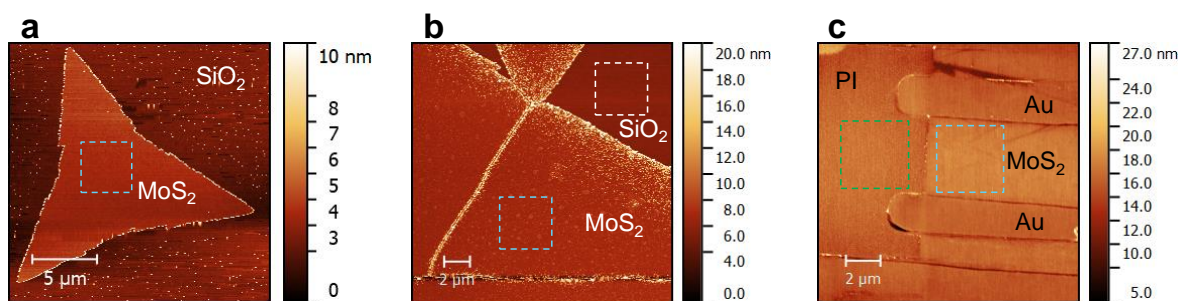


Supplementary Fig. 3 | Optical analysis of mono- vs. multilayer regions of MoS₂. **a**, Continuous MoS₂ film in chip center of a *Type A* device after transfer, scale bar: 50 μm. **b**, Non-continuous MoS₂ region in chip edge of a *Type A* device after transfer, scale bar: 50 μm. **c**, Etched MoS₂ film of a *Type B* device before transfer, scale bar: 20 μm. **d**, Etched MoS₂ film of a *Type B* device after transfer, scale bar: 20 μm.

(Supplementary Fig. 3c,d). Thus, for micron-scale devices we can assume that the channel will be mostly composed of monolayer MoS₂ (including multilayer islands), while most nanoscale channels will likely be monolayers with the occasional chance of continuous bilayers in the channel gap.

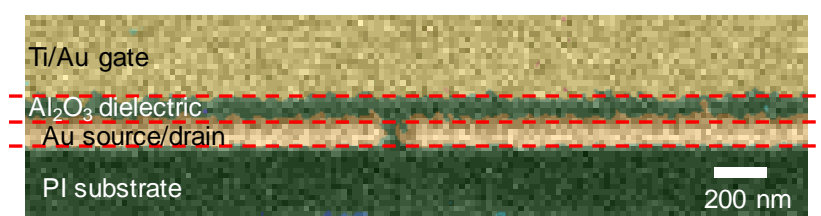
2. Surface analysis before and after transfer

To investigate the surface morphology of the MoS₂ covered regions before and after transfer, we performed atomic force microscopy (AFM). We find that the as-grown MoS₂ has a root-mean-square (rms) roughness of 0.18 – 0.45 nm depending on growth run and sample location, which is comparable to or slightly larger than the nominal SiO₂ roughness (Supplementary Fig. 4). In addition, we have also measured the roughness after transfer and capping with 35 nm Al₂O₃ (evaporated Al seed layer + atomic-layer deposition as described in Methods), which yielded a roughness of 0.39 nm on the MoS₂ covered region and 0.44 nm where MoS₂ was etched prior to transfer. This confirms that the extremely smooth MoS₂ surface is preserved even after transfer. In addition, the AFM reveals that the height difference between MoS₂ and Au surfaces is less than 2 nm which confirms that the 45 nm thick contacts are embedded in the substrate and topography is effectively eliminated. This is further visualized in the cross-section SEM image after completed device fabrication in Supplementary Fig. 5, where Al₂O₃ and Au cover the contacts and channel without any “steps” in surface topography.



Note: Al_2O_3 capped across the entire area.

Supplementary Fig. 4 | Atomic Force Microscopy (AFM) of **a**, a single MoS_2 triangle on SiO_2/Si with a root mean square (rms) roughness of 0.18 nm measured in region of light blue dashed box, **b**, an MoS_2 on SiO_2/Si region of coalescing grains with rms roughness of 0.45 nm for MoS_2 (light blue dashed box) and 0.23 nm for the bare SiO_2 surface (white dashed box), and **c**, the MoS_2 and Au structures on polyimide after transfer and alumina capping (on the entire area) with rms roughness of 0.39 nm on the region with MoS_2 (light blue dashed box) and of 0.44 nm on the region where MoS_2 was etched (green dashed box).



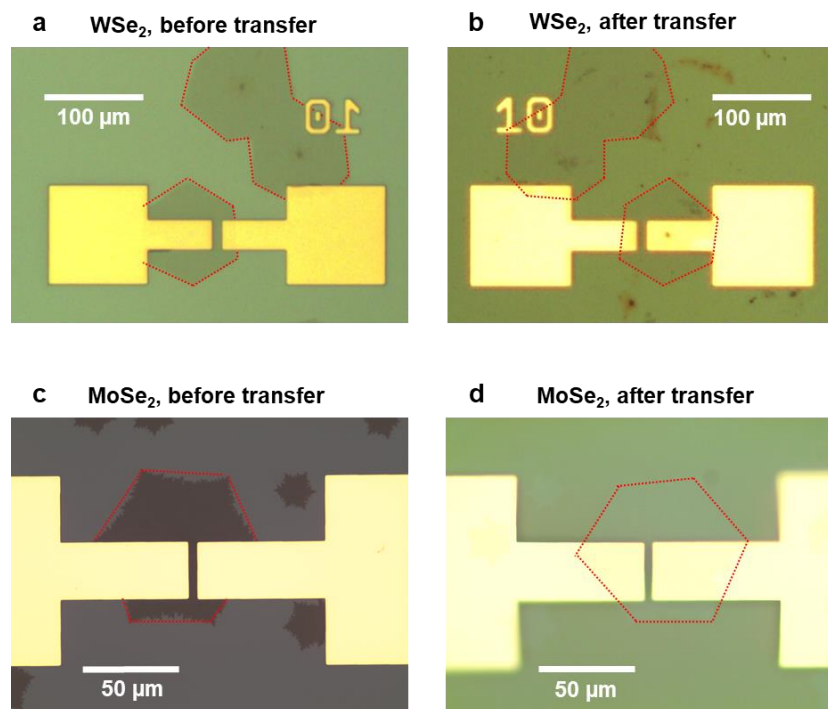
Supplementary Fig. 5 | Scanning-electron microscopy (SEM) cross-section of a ~ 100 nm long channel MoS_2 transistor, colorized version of Fig. 3a. Red dashed lines show the source and drain electrodes are embedded in the PI, and no “steps” in surface topography can be discerned.

3. Optical microscope images for WSe_2 and MoSe_2 before and after the transfer process

Supplementary Fig. 6a,c displays the hexagonally shaped WSe_2 and MoSe_2 crystal grains grown on SiO_2/Si substrates after the patterning of source/drain metal contacts, and *before* the transfer. As visible here, the Au contacts are on top of the TMDs. When the polyimide (PI) is applied on top, it uniformly covers and embeds the contacts. After releasing the PI together with metals and TMDs from the SiO_2/Si substrates (main text Fig. 1b), the substrate is flipped over as visible in the numbering (“10”) when comparing Supplementary Fig. 6a,b. This also leads to a reversal of the material stack, where the TMDs are on top of Au/PI or PI, as visible in Supplementary Fig. 6b,d.

4. Raman spectroscopy and Photoluminescence measurements before and after transfer process

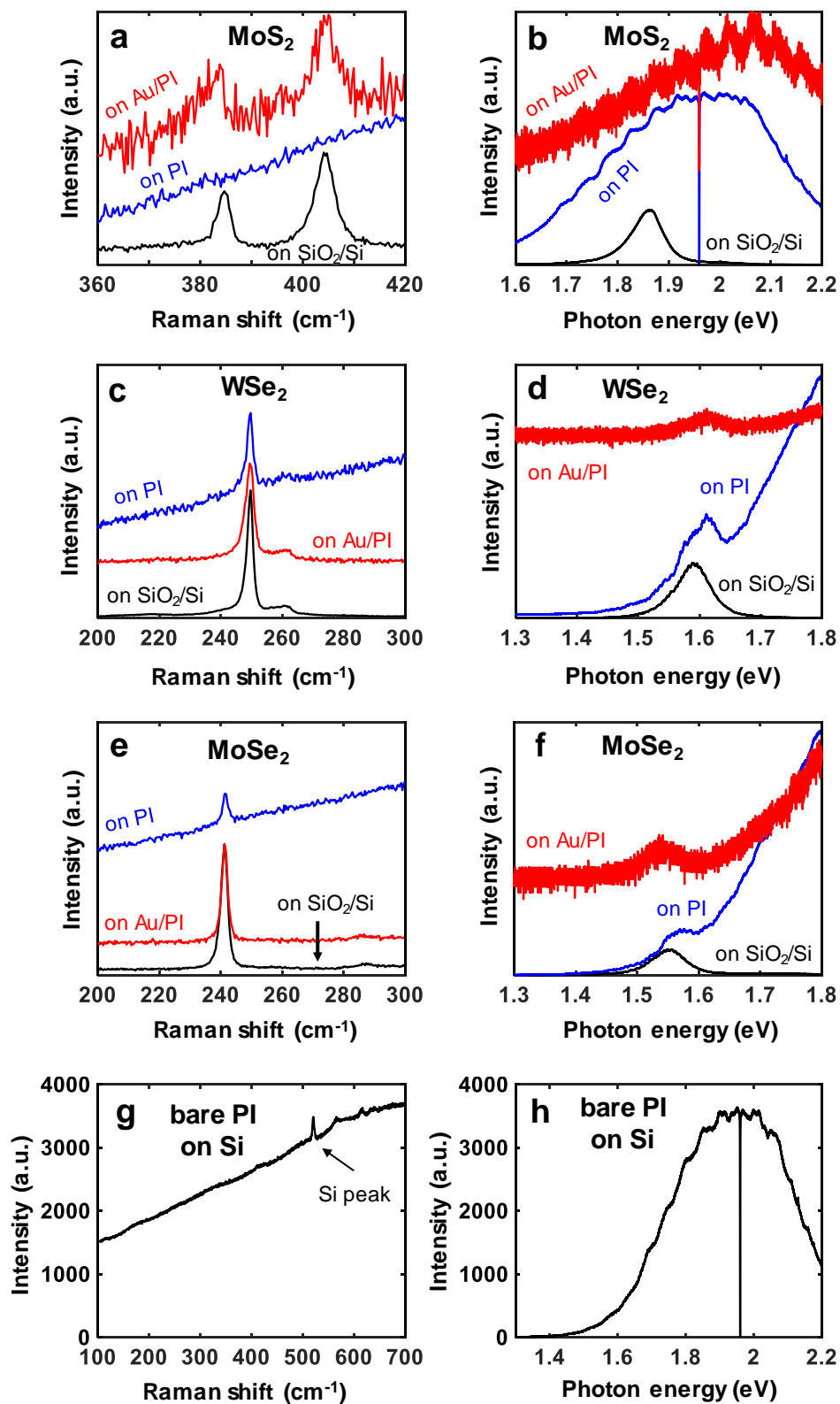
The different TMDs were monitored with Raman spectroscopy and photoluminescence (PL) throughout the transfer process to investigate any changes in material properties. Supplementary



Supplementary Fig. 6 | Microscope images of WSe₂ and MoSe₂ with patterned Au metal electrodes. a, WSe₂ on SiO₂/Si before transfer. **b,** WSe₂ on polyimide (PI) after transfer. **c,** MoSe₂ on SiO₂/Si before transfer. **d,** MoSe₂ on PI after transfer.

Fig. 7a-f display the spectra for MoS₂, WSe₂ and MoSe₂ before and after transfer. Because we have deposited and patterned metal contacts before the transfer, released all materials together, and flipped the flexible PI substrate, we were able to measure the TMDs after transfer on the metal surface and on the PI surface.

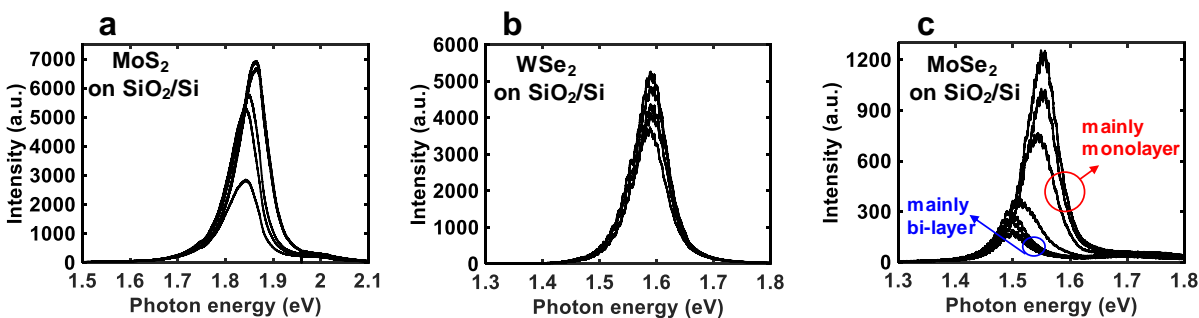
We observed that the measurements directly on PI (without a metal in between the TMD and PI) have a broad background signal, which is absent on the SiO₂/Si substrates and on Au surfaces. This background signal is in the range where we expect the vibrational modes of the TMDs, and there is, for instance, a significant overlap with the PL energy maximum of monolayer MoS₂ (Supplementary Fig. 7b). The Raman and PL measurements for bare PI (on Si) are shown in Supplementary Fig. 7g,h for comparison. Because of this background signal, the MoS₂ Raman and PL peaks are buried and not visible in our measurements on PI. However, the peaks of WSe₂ and MoSe₂ on the PI surface can be resolved (Supplementary Fig. 7c-f). We note that a Raman laser with shorter wavelength could possibly help to reduce the background signal from PI and improve detection of TMDs.⁶⁰ Further, the insertion of Au between PI and the TMD suppresses this background signal and enables the detection of the Raman signature of all three TMDs.



Supplementary Fig. 7 | Raman (left column) and photoluminescence (right column) spectra. a,b, MoS_2 . c,d, WSe_2 . e,f, MoSe_2 . g,h bare polyimide (PI) on silicon.

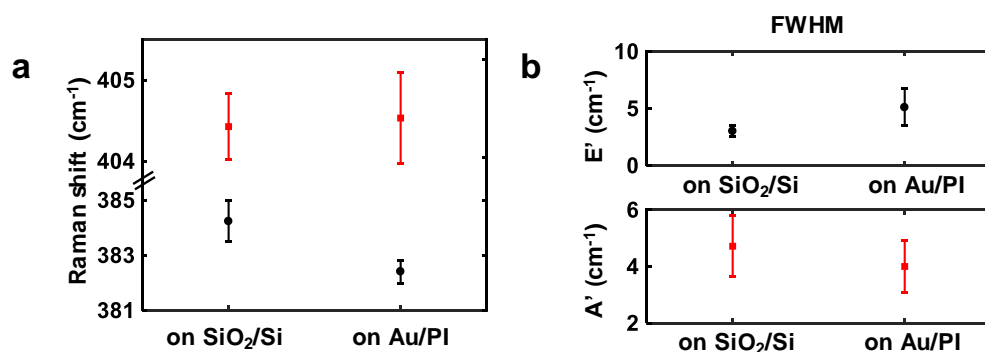
We find that the PL peaks for WSe₂ and MoSe₂ can be detected on PI and Au/PI despite the strong PL quenching that is known to appear on Au surfaces.^{33,34} The PL peak energies of MoS₂, WSe₂ and MoSe₂ are ~1.86 eV, ~1.59 eV and ~1.54 eV, all indicating monolayer thickness.^{29,61-63} While these results were consistent for MoS₂ and WSe₂ across the substrate, we found that MoSe₂ had areas with monolayers and bilayers (~50%) (Supplementary Fig. 8), where the PL peak is shifted towards ~1.50 eV and its intensity is significantly reduced. The noticeable spread in PL energies for MoS₂ can be attributed to a variety of effects such as nanoscale bilayer regions^{27,28} or small local variations in strain or doping. For MoSe₂, however, we find two sets of PL energy peak positions, which indicate that some areas mainly consist of monolayers and some mainly of bilayers (~50% each).^{29,61}

Changes in the Raman and PL spectra before vs. after transfer can be interpreted as strain release effects or phonon interactions with the bottom surfaces (PI or Au), as will be discussed in the following. For MoS₂ on Au, we find that the E' peak shifts by about -1.8 cm⁻¹ and its full-width-half-maximum (FWHM) increases, whereas the A'₁ peak does not change discernably (see Supplementary Fig. 9), which has been observed for non-transferred Au/MoS₂ stacks and thus cannot be correlated with the transfer process. Possible mechanisms for this E' peak shift and broadening can be tensile strain induced from the Au deposition^{64,65} or electron-phonon interactions due to Au plasmons.^{66,67} For WSe₂, the changes in the Raman and PL spectra are small (Supplementary Fig. 10). The minor shifts in the PL peak position and Raman E' peak of about +0.02 eV and -0.1 to -0.2 cm⁻¹, respectively cannot be consistently correlated with any strain release during transfer,⁶⁸ and may be related to small effects from interactions with the substrate.⁶⁹ It is difficult to deduce any strain effects from PL and Raman for MoSe₂, due to small changes and existence of mono- and bilayers adding uncertainty to the Raman and PL analysis. Still, the results suggest the possibility of slight strain changes in tensile and compressive directions on Au/PI and PI surfaces, respectively (see Supplementary Fig. 11).⁷⁰⁻⁷²

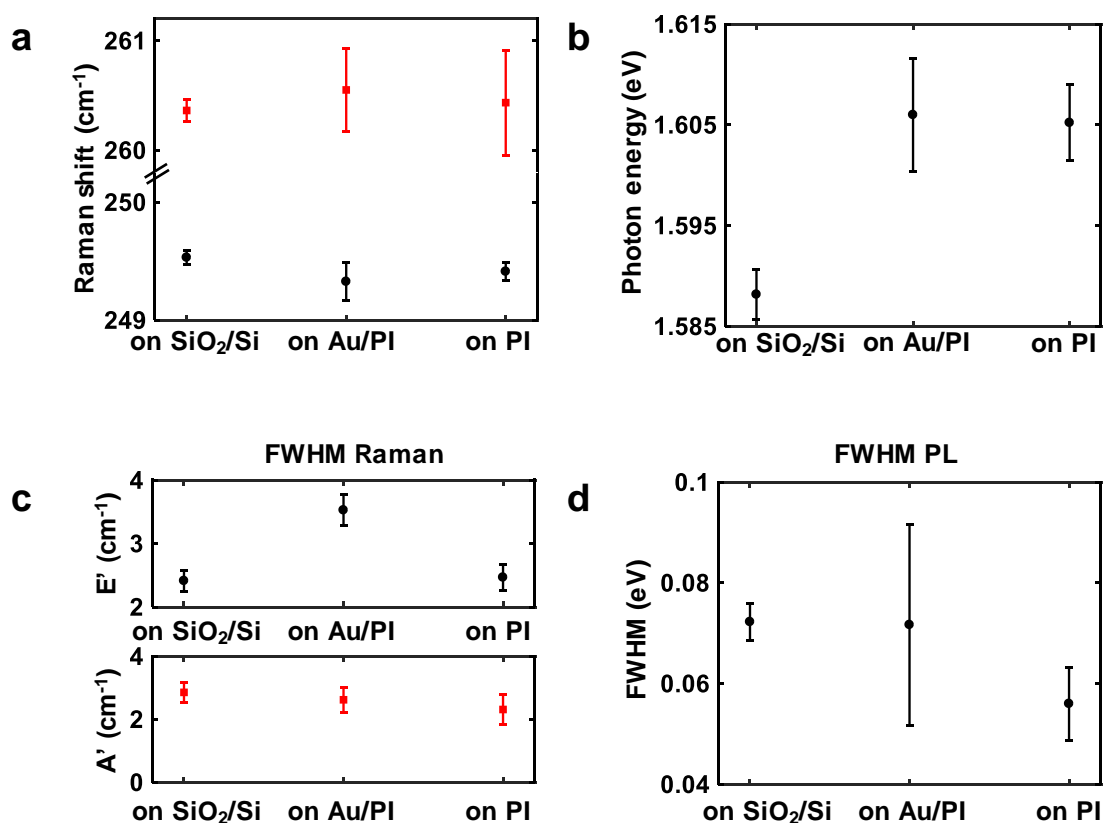


Supplementary Fig. 8 | PL measurements before transfer of **a**, MoS₂, **b**, WSe₂ and **c**, MoSe₂.

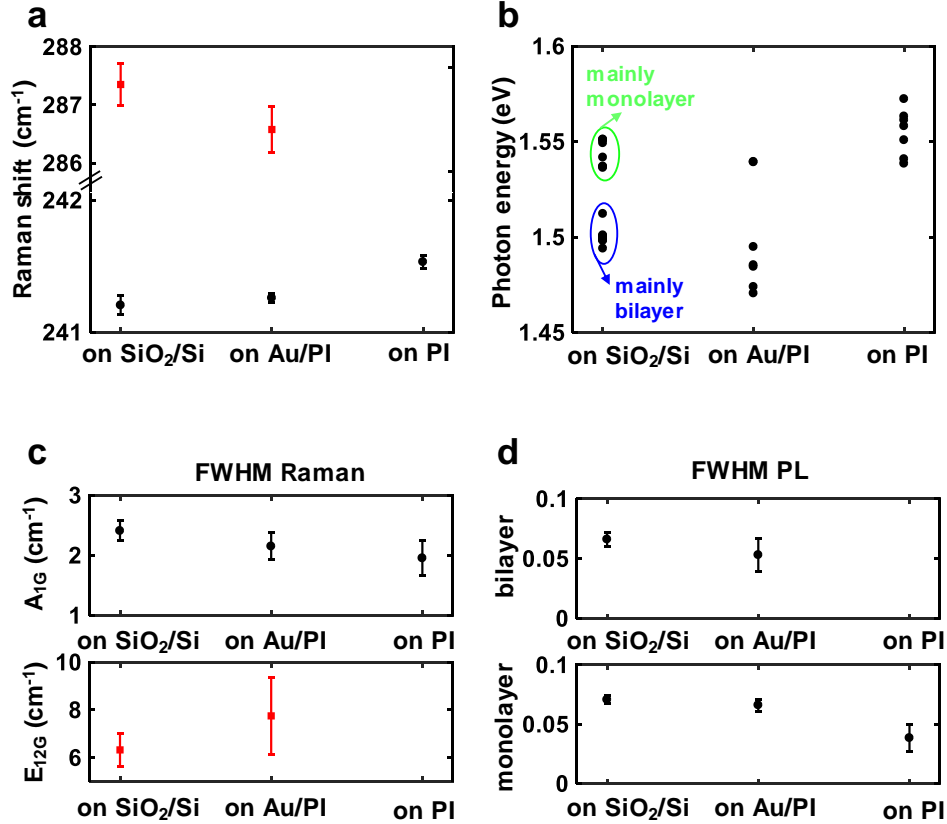
Overall, the FWHM of the Raman and PL peaks for all the TMDs do not increase except on Au electrodes, where previously discussed plasmonic effects could be the leading cause. This indicates that the disorder, which would be affected by crystal grain size or defect density, in the materials is not increased throughout the transfer process.^{73,74} This conclusion is also supported by the good electrical



Supplementary Fig. 9 | Averaged Raman (over ~5 spots on the same chip) **a**, peak positions and **b**, Full-width-half-maximum (FWHM) of MoS₂ before transfer (as-grown, on SiO₂/Si substrate) and after transfer (on Au/PI).



Supplementary Fig. 10 | Averaged (over ~5 spots on the same chip) **a**, Raman and **b**, photoluminescence (PL) peak positions of WSe₂ before and after transfer. Averaged full-width-half-maximum (FWHM) for **c**, the Raman and **d**, the PL measurements.



Supplementary Fig. 11 | **a**, Averaged Raman (over ~5 spots on the same chip) and **b**, photoluminescence (PL) peak positions of MoSe₂ before and after transfer. Averaged full-width-half-maximum (FWHM) for **c**, the Raman and **d**, the PL measurements (~10 spots across two chips). Note, missing data e.g., for the Raman E_{12G} peak on PI means that these peaks could not be detected on that particular surface.

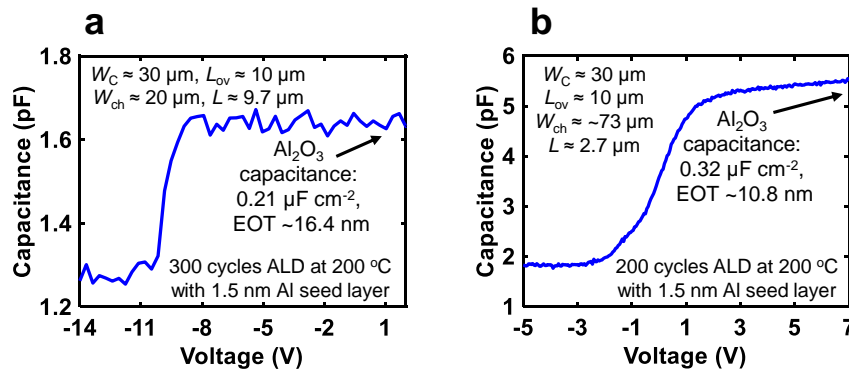
properties, which are comparable on the materials after transfer with those before transfer (i.e. on rigid SiO₂/Si substrates) from previous studies using the same CVD material type.^{27,28,35}

5. Mobility, Gate Capacitance, and Threshold Voltage Extraction

We performed the extraction of the extrinsic field-effect mobility $\mu_{FE,ext}$ and threshold voltage V_T from the g_m maximum based on the following equation (valid for small drain-source voltages V_{DS}):

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{\mu_{FE,ext} C_{ox} V_{DS} W}{L},$$

where the I_D plotted vs. V_{GS} can be fitted linearly to obtain $\mu_{FE,ext}$. Furthermore, the intercept with the V_{GS} axis yields V_T .^{75,76} The channel width W and the channel length L are given by the device geometry. The gate oxide capacitance per unit area (C_{ox}) is determined by connecting source and drain of the



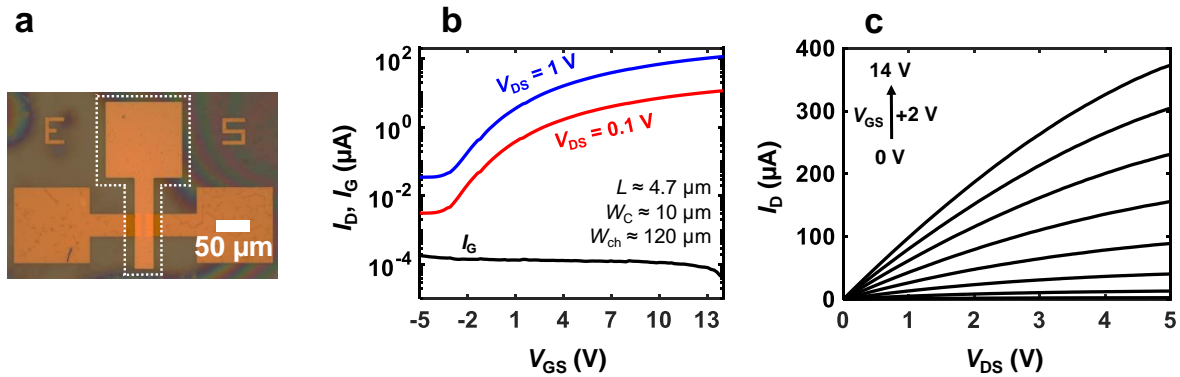
Supplementary Fig. 12 | Measured capacitance-voltage (C - V) characteristics of flexible TMD-FETs. Typical C - V for **a**, MoS₂ FETs and **b**, MoSe₂ and WSe₂ FETs, where the calculated Al₂O₃ capacitance density and equivalent oxide thickness (EOT) represent average values (~ 5 devices). L_{ov} is the overlap length between the gate electrode and the source/drain electrodes.

transistors to ground, and applying a voltage to the gate electrode. We then perform small-signal capacitance-voltage (C - V) measurements where the direct-current (dc) voltage is swept while applying an alternating-current (ac) voltage with an amplitude = 100 mV and frequency = 20 kHz. The results for Al₂O₃ gate dielectrics (including 1.5 nm Al seed layer) deposited in 300 cycles (MoS₂ FETs) and 200 cycles (WSe₂ and MoSe₂ FETs) are shown in Supplementary Fig. 12a and b, respectively.

As all transistors are n -channel devices, we estimate the capacitance of the Al₂O₃ gate dielectrics at positive bias voltage (when the channel is in accumulation) by dividing the measured capacitance (Supplementary Fig. 12) with the overlap area of the gate with the source, drain, and semiconductor channel.³⁶ For MoS₂ FETs the extracted $C_{ox} \approx 0.21 \mu\text{F cm}^{-2}$ or an equivalent oxide thickness (EOT) $\sim 16.4 \text{ nm}$, and for WSe₂ and MoSe₂ FETs we obtain $C_{ox} \approx 0.32 \mu\text{F cm}^{-2}$ or EOT $\sim 10.8 \text{ nm}$. Estimating the relative dielectric constant ϵ_r from C_{ox} and the Al₂O₃ thickness obtained by ellipsometry, we find $\epsilon_r \approx 7$ -8, which is in the expected range.^{77,78} Note, the ellipsometric thickness of 200 cycles and 300 cycles of atomic-layer deposited (200°C) Al₂O₃ measured on silicon is around 22 nm and 35 nm, respectively. However, for the transistor capacitance the 1.5 nm oxidized Al seed layer adds to the overall thickness, while the optical lithography and lift-off process of the top (gate) electrode exposes the Al₂O₃ to the basic photoresist developer which can etch the material, thus slightly reducing its thickness.

6. Flexible MoS₂ Field-Effect Transistors of Type A

Supplementary Fig. 13 displays a top-down optical microscope image and the electrical characteristics of a flexible MoS₂ field-effect transistor (FET) of Type A with $4.7 \mu\text{m}$ channel length. The device exhibits an extrinsic field-effect mobility $\mu_{\text{FE,ext}} \sim 14.2 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, on-current $I_D \sim 5.5 \mu\text{A } \mu\text{m}^{-1}$ at a drain-

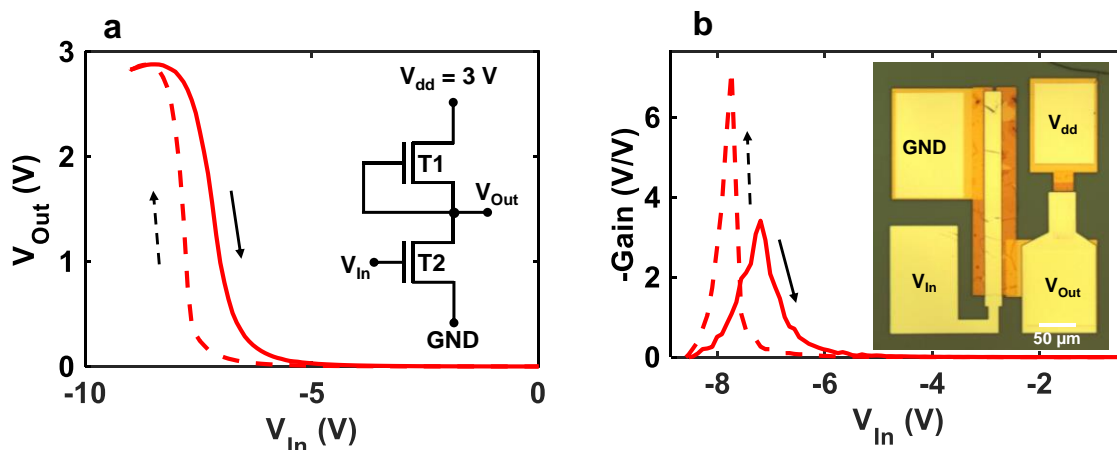


Supplementary Fig. 13 | MoS₂ field-effect transistors (FETs) of Type A. **a**, Top-down optical microscope image, white dotted line marks the outline of the MoS₂ area. **b**, Measured transfer characteristics. Red and blue lines represent drain current, I_D . **c**, Output characteristics.

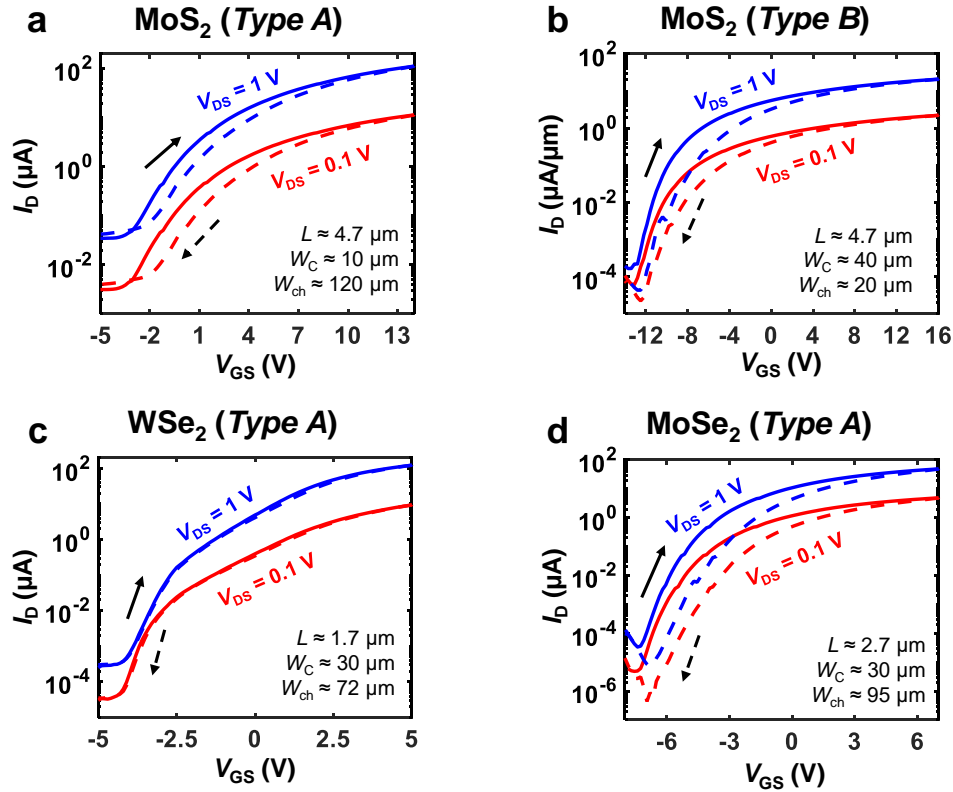
source voltage $V_{DS} = 1$ V, threshold voltage $V_T = 3.9$ V, minimum subthreshold swing $SS \approx 1.7$ V dec⁻¹ and on/off ratio $\sim 3.6 \times 10^3$. Note that $\mu_{FE,ext}$ and I_D have been corrected for current spreading, which is described in Section 15 below.

7. Flexible MoS₂ Inverter based on Type B device fabrication process

The fabrication process for Type B devices further facilitates the realization of circuits because MoS₂ is already defined before gate dielectric deposition and the second metallization, which simplifies connecting bottom and top metallization layers. For instance, these are useful for practical circuits, where the gates and source/drain contacts of some transistors need to be connected (see inset of Supplementary Fig. 14a). Supplementary Fig. 14 shows the characteristics of a proof-of-concept flexible inverter realized with two *n*-type MoS₂ transistors.



Supplementary Fig. 14 | Flexible inverter with Type B MoS₂ transistors. **a**, Transfer characteristic of the inverter. Inset shows the schematic circuit diagram with transistors T1 ($W_{ch}/L \approx 20/39.7$ μm) and T2 ($W_{ch}/L \approx 300/4.7$ μm) **b**, Gain of the inverter shown in a. Inset shows an optical microscope image of the inverter after fabrication.



Supplementary Fig. 15 | Hysteresis in flexible transition metal dichalcogenide field-effect transistors. a, MoS₂ (Type A). b, MoS₂ (Type B). c, WSe₂ (Type A). d, MoSe₂ (Type A).

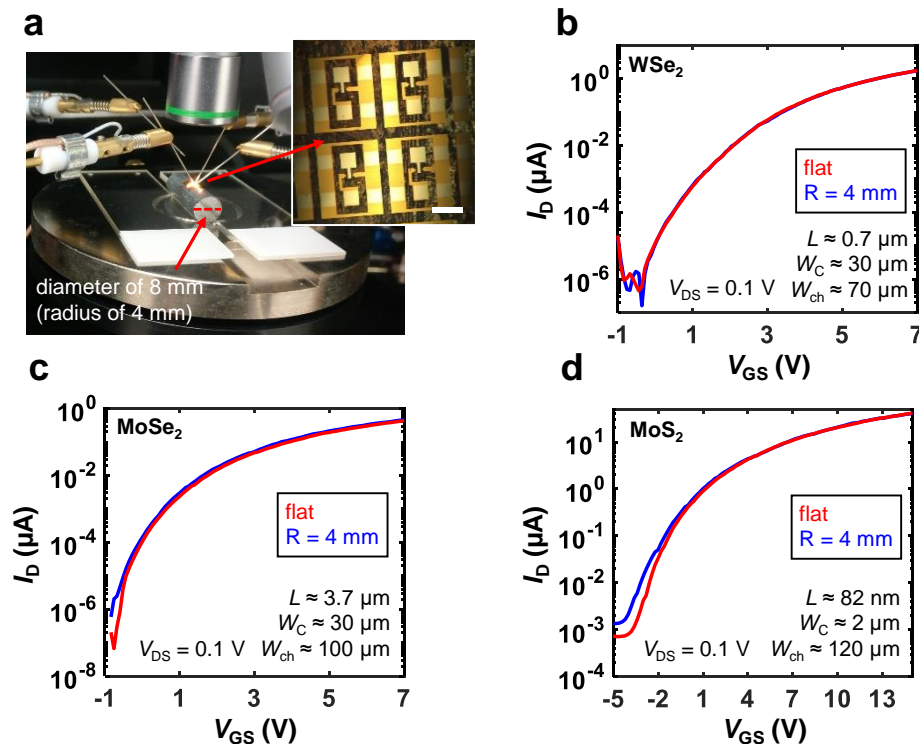
8. Hysteresis

Comparing hysteresis³⁷ for *Type A* and *Type B* devices, we find similar maximum values of ~ 1.2 V for MoS₂ FETs, which indicates that the additional etch step before transfer does not deteriorate the TMD interfaces (Supplementary Fig. 15a,b). The WSe₂ FET displays low hysteresis ~ 0.1 V (Supplementary Fig. 15c), and the MoSe₂ FET has maximum hysteresis of ~ 1.6 V (Supplementary Fig. 15d).

9. Bending of flexible TMD FETs

Flexible electronics need to remain unaltered when mechanically deformed, for instance, by bending the substrate. While the ductility of materials matter for the maximum strain that flexible electronics can sustain,⁷⁹ the easiest way to minimize impacts of strain on flexible electronic devices is to minimize the substrate thickness. The strain at a given bending radius can be approximated as:⁸⁰

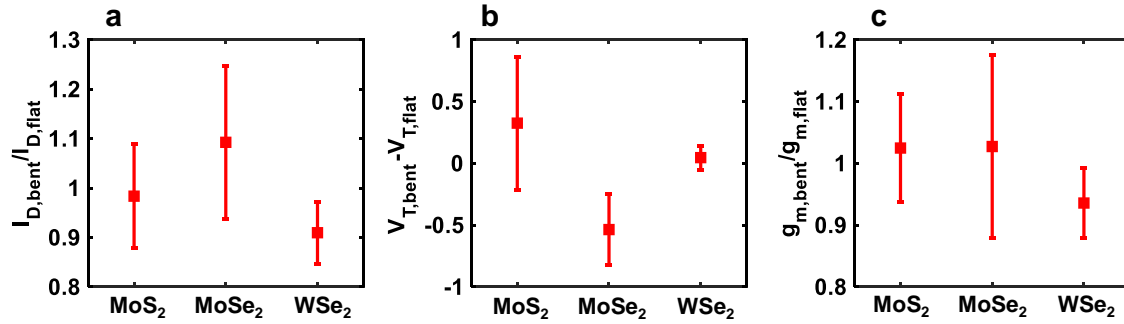
$$\text{strain} = \frac{d}{2r},$$



Supplementary Fig. 16 | Mechanical bending of flexible TMD-FETs. **a**, Photograph and microscope image (scale bar: 200 μ m) of the measurement setup where the FETs are bent to a tensile radius of 4 mm. Measured transfer characteristics of **b**, WSe₂ (Type A), **c**, MoSe₂ (Type A) and **d**, MoS₂ (Type A). All show no significant changes on substrate bending at the 4 mm radius.

where d is the substrate thickness and r is the radius of curvature. Thus, by minimizing d to a few micrometers, the strain at common bending radii on the order of millimeters is minimized. We show this by using a ~ 5 μ m thick PI substrate and bending it to a radius of 4 mm, which results in $\sim 0.063\%$ of strain. Consequently, the electrical characteristics of the TMD FETs remain visually unaltered in this condition as shown in Supplementary Fig. 16.

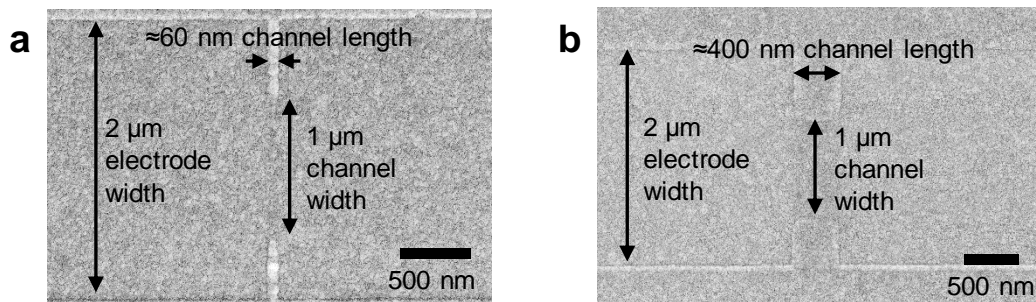
For a detailed quantitative evaluation, we have further analyzed transistor parameters such as drain current I_D , threshold voltage V_T and transconductance g_m (see Supplementary Fig. 17). Average I_D and g_m changes remain within 10% of the flat state values and absolute V_T shifts are mostly < 0.5 V. Given that the applied strain is low even at $r = 4$ mm, we conclude that no systematic correlations of strain with device performance parameters can be deduced from these results and we successfully confirmed the bending stability of our devices.



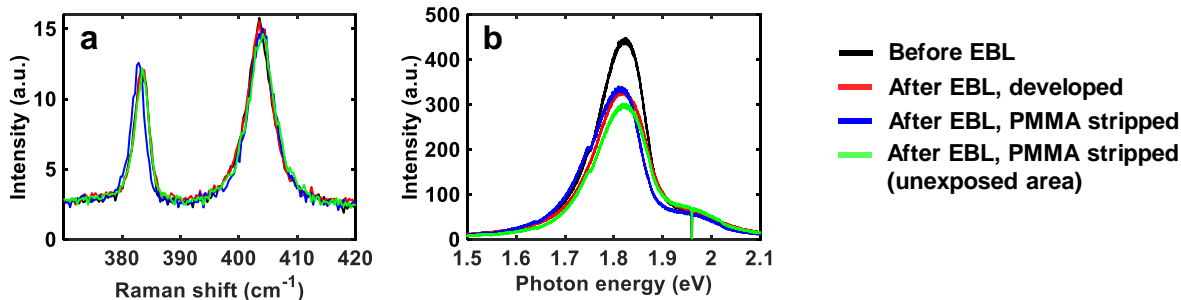
Supplementary Fig. 17 | Quantitative analysis of TMD transistors under bending to a radius of 4 mm. For MoS₂, MoSe₂ and WSe₂, displayed values represent the average and standard deviation of 12, 6 and 3 devices, respectively. a, Maximum drain current I_D under bending normalized by its value in flat condition. b, Threshold voltage shift $V_{T,bent} - V_{T,flat}$. c, Maximum transconductance g_m normalized by its value in flat condition.

10. SEM images of transistor channels fabricated with electron-beam lithography (EBL)

We verified the channel dimensions in our transistors by performing scanning-electron microscopy (SEM), which reveals the channel lengths and widths even after the top gate metal is deposited. Supplementary Fig. 18 shows two exemplary *Type B* devices with channel lengths of ~ 60 nm and ~ 400 nm. Note that the surface consists of Au across the whole area displayed since everything is covered with the top gate. Nevertheless it is possible to discern the edges where the MoS₂ has been etched. The MoS₂ etch mask consists of 2 μ m wide metal leads (left and right) and photoresist covering the 1 μ m wide channel region, which results in no discernable edge across the MoS₂ on Au and the MoS₂ in the channel. This is consistent with the absence of “steps” in surface topography from the SEM cross-sections (Supplementary Fig. 5) and AFM images (Supplementary Fig. 4). In our EBL process, the intended channel length was 50 nm, and after evaluating Supplementary Fig. 18a, we



Supplementary Fig. 18 | SEM top-view images of *Type B* transistors. a, Device with a channel length ~ 60 nm. b, Device with a channel length ~ 400 nm.

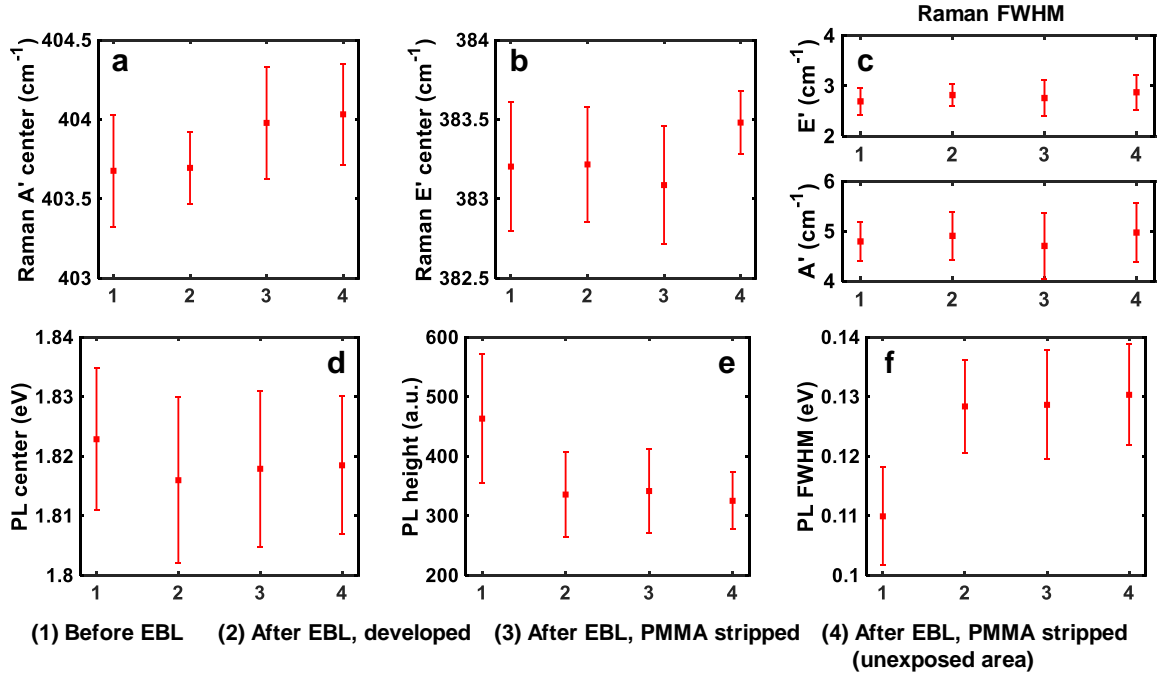


Supplementary Fig. 19 | Optical material analysis of MoS₂ throughout an electron-beam lithography (EBL) process involving spin-coating and stripping of poly(methyl methacrylate) (PMMA). a, Raman spectra. b, Photoluminescence spectra.

estimate its actual length is 63 ± 7 nm. Analyzing 9 devices with sub-micron channels we find that on average the channel length is ~ 12 nm longer than intended in our device layout. Thus, we have corrected our extractions and evaluations on devices fabricated by EBL by $\Delta L = +12$ nm. Similarly, we applied $\Delta L = -0.3$ μm for devices fabricated by optical lithography based on SEM measurements.

11. Electron Beam Lithography on top of MoS₂

Previous reports have indicated that MoS₂ could be damaged by highly energetic electron beams which cause strain and defect formation.⁸¹⁻⁸⁴ We investigated this for our EBL process (details in the Methods section) performing Raman and PL measurements before and after the electron beam exposure and development of the poly(methyl methacrylate) (PMMA) layer that was used for the lift-off of the later deposited source/drain metal. Supplementary Fig. 19 displays exemplary Raman and PL spectra, while Supplementary Fig. 20 provides the analysis of Raman and PL peak center shifts as well as the changes in the intensity and FWHM of the PL spectra. We found negligible differences in the Raman spectra. The slight reduction in the PL intensity (Supplementary Fig. 19b) occurs independently of the exposure to the electron beam, and may be caused by PMMA residues or minor effects from processing and aging of the material. Thus, we conclude that here we do not cause significant damage during the EBL process, which may have been due to our 200 nm thick high molecular weight (950K) PMMA layer on top that should reduce the impact energy and dosage of electrons that hit the MoS₂. The other parameters of our EBL process and the device fabrication can be found in the Methods section.



Supplementary Fig. 20 | Averaged optical material analysis of MoS₂ during electron-beam lithography (EBL) with spin-coating and stripping of poly(methyl methacrylate) (PMMA). a, Raman A' peak center. b, Raman E' peak center. c, Averaged full-width-half-maximum (FWHM) of the Raman peaks. d, Photoluminescence (PL) peak center. e, PL peak height. f, PL FWHM.

12. Temperature Rise Estimates

We estimate the MoS₂ and PI substrate temperature rises in a short-channel ($L \sim 82$ nm, $W_C = 2$ μ m) Type A MoS₂ device. This particular “hero” device was chosen because it achieved the highest power dissipation, and is therefore expected to reach the highest temperatures during device operation. The operating point simulated is $V_{GS} = 16$ V, $V_{DS} = 1.2$ V and $I_D = 1.225$ mA, which corresponds to the highest power (1.47 mW) demonstrated in Fig. 3f. In order to account for interface thermal resistances and various heat paths and current spreading, we perform 3D steady-state thermal finite element method (FEM) simulations, with the device geometry shown in Supplementary Fig. 21a. The 5 μ m thick PI substrate is attached to a heat sink at $T_0 \approx 20^\circ\text{C}$ via photoresist (SPR 3612, Shipley), which serves as the thermal interface material. For simulations, a thermal contact resistance of 0.1 K \cdot cm²/W was assumed at the bottom of the PI substrate (typical of contact resistances in device packaging⁸⁵), although the exact value has little effect on simulated peak temperatures in this case, because its contribution to the total thermal resistance is much less than the thermal resistance of the PI substrate and the device thermal circuit. The thermal conductivities of the materials used in the simulations and the thermal boundary resistances (TBR) of material pairs are given in Supplementary Table 1.

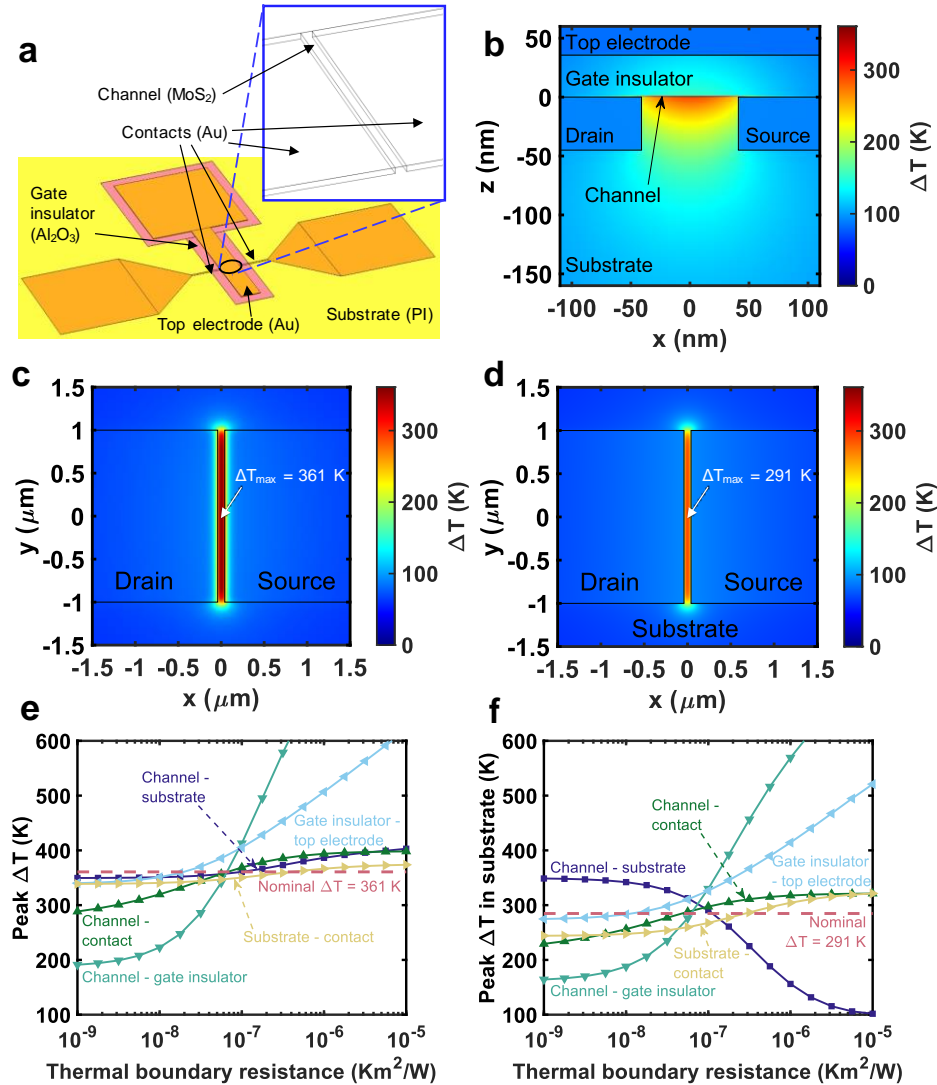
Material	Thermal conductivity (Wm ⁻¹ K ⁻¹)	Material interface	Thermal boundary resistance (Km ² /GW)
MoS ₂ ⁸⁶	20 (in-plane)	MoS ₂ – polyimide ⁸⁷	100
Polyimide (PI) ⁸⁸	0.2	MoS ₂ – Au ⁸⁹	67
Au ⁹⁰	150	MoS ₂ – Al ₂ O ₃ ⁸⁹	67
ALD Al ₂ O ₃ ^{91,92}	2.5	Au/Ti – ALD Al ₂ O ₃ ⁹²⁻⁹⁵	20
		Au – polyimide ⁹⁶	400

Supplementary Table 1: Nominal values of material thermal properties in the simulations. Some thermal boundary resistance (TBR) values not available in literature were approximated by TBRs for pairs of similar and/or better-studied materials, using the larger estimates to model a worst-case scenario. Actual values can vary depending on the material/interface quality and deposition conditions. For Au, the thermal conductivity of films with comparable thickness (not bulk) is used.⁹⁰ For PI and Al₂O₃, the thermal conductivities above room temperature (in the 100-200°C range) are used.

To estimate the temperature rise, we first obtain the current distribution in the device. With $V_{DS} < V_{GS} - V_T$, the device was assumed to be in the linear region, where the MoS₂ film is characterized by a uniform sheet resistance and the current density is symmetric about the center of the device. With an assumed contact resistance of 400 $\Omega \cdot \mu\text{m}$ and a contact transfer length of 50 nm (in this “hero” device), 2D electrical simulations were performed as described in Supplementary Section 15 to account for current spreading, and a mobility of 25 cm²V⁻¹s⁻¹ was found to yield the correct device current. The power dissipated per unit area in the channel and across the contact interface were calculated from the simulated current densities and potential drops across the contact-MoS₂ interfaces. This power distribution was then used in the thermal simulation with the complete 3D geometry.

With the nominal thermal properties specified in Supplementary Table 1, the Supplementary Fig. 21 shows the 2D temperature rise distributions (b) in a vertical device cross section, (c) within the MoS₂ film and (d) immediately below the MoS₂ film, showing temperatures in the upper surface of the PI substrate and the Au contacts. We determine a peak temperature rise $\Delta T \sim 361$ K in MoS₂ and 291 K in PI (The difference between the two is due to the TBR between MoS₂ and PI.). Because TBRs across interfaces depend strongly on materials and the interface quality, the TBRs in the actual device might differ from the values given in Supplementary Table 1. Thus, we performed sensitivity analysis of the peak MoS₂ and PI temperature rise on the TBRs (for all interfaces), in Supplementary Fig. 21e,f.

Supplementary Fig. 21e shows that peak device temperatures are most sensitive to channel-gate insulator (MoS₂-Al₂O₃) and gate insulator-top electrode (Al₂O₃-Ti/Au) TBRs, which indicates that TBRs that control heat flow into the gate stack have the greatest influence. This also indicates the heat



Supplementary Fig. 21 | Thermal simulations. **a**, Simulated *Type A* device geometry. Inset: closer view of the channel, with the top gate stack not shown. **b**, Cross section of temperature rise along the direction of current flow. Note the gate has significant overlap with the source/drain. **c**, Top view of temperature rise in the MoS₂ channel, where the highest temperatures occur. **d**, Top view of temperature rise at the top of the PI substrate and Au contacts, just below the MoS₂ channel. **e**, The variation of the device peak temperature rise as a function of the TBR of each material pair. **f**, The variation of the highest temperature rise in the PI substrate as a function of the TBR of each material pair. In **e** and **f** the horizontal dashed lines indicate the peak temperature rise, and the intersection of each curve with this line occurs at each nominal TBR value.

generated in the device spreads (at first) mainly through the gate stack, which has substantial overlap ($\sim 10 \mu\text{m}$) with the source/drain electrodes. As the heat sink is at the bottom of the PI substrate, after spreading via the gate insulator and top gate, the heat flows back down into PI via MoS₂ and the Au contacts. We note that only $\sim 10\%$ of the heat flows from MoS₂ directly into the PI (the channel-substrate TBR), thus even if the PI surface were severely compromised (e.g. due to heating during

device operation), the device could continue to function by dissipating heat into the gate and contacts. The PI glass transition temperature⁹⁷ is 360°C and the decomposition temperature is 620°C. Thus, for the nominal properties in Supplementary Table 1, these devices have additional headroom to operate at higher power, thanks to heat spreading through their gate and source/drain electrodes.

13. Additional *Type A* Device Data and Overall Variability

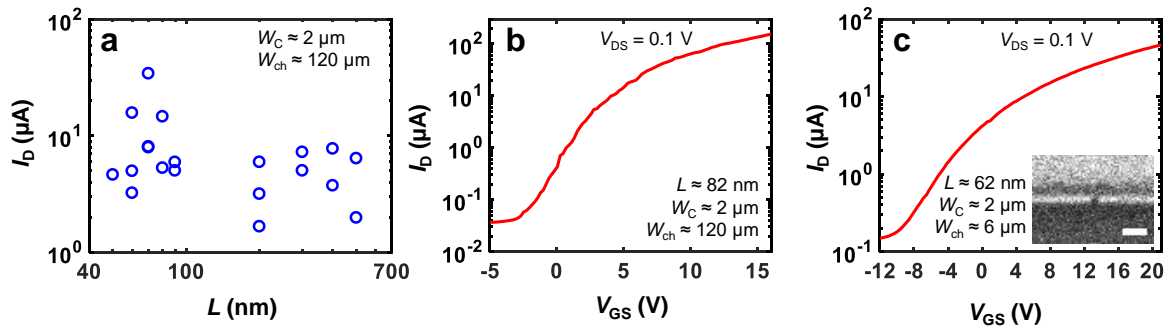
The variability of I_D for *Type A* devices shows a similar distribution compared to devices of *Type B* (compare Supplementary Fig. 22a with Fig. 3d). The transfer characteristic of the device with the highest on-current is displayed in Supplementary Fig. 22b. The shortest channel lengths which we realized were ~60 nm and an exemplary electrical characteristic and scanning-electron microscopy cross-section are shown in Supplementary Fig. 22c.

In Supplementary Fig. 23 we display the V_T histogram for all MoS₂ devices measured. Academic fabrication and growth variations (e.g., variations in S vacancy concentration^{98,99}) cause V_T variability, which could be much improved with industrial process optimization (beyond the scope of this work).

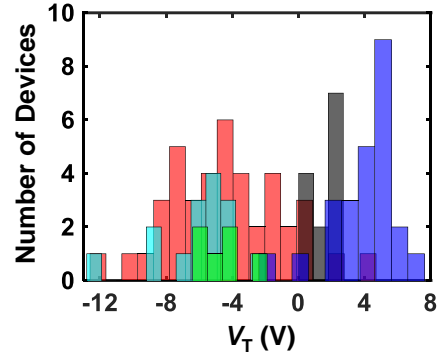
14. Drain current vs channel length in flexible MoS₂ FETs and Modeling

The drain current I_D that is obtained when probing a short-channel FET typically has contributions from the channel resistance R_{ch} and contact resistance R_C , which makes the accurate extraction of the intrinsic mobility μ_{FE} difficult. Furthermore, since short-channel devices can be contact dominated, an estimation of R_C is also important. Taking into account R_{ch} and equal source and drain R_C we can estimate the overall resistance R_{tot} (all normalized by device width W , in units $\Omega\cdot m$) as follows:

$$R_{tot}/W = 2R_C/W + R_{ch}/W.$$



Supplementary Fig. 22 | MoS₂ *Type A* transistors. **a**, Drain current I_D vs. channel length at a drain-source voltage $V_{DS} = 0.1$ V and an overdrive voltage $V_{GS} - V_T = 8$ V. **b**, I_D vs. V_{GS} of the device with the highest on-current (also see Fig. 3f). **c**, Electrical characteristic of a *Type A* flexible MoS₂ field-effect transistor with the shortest channel length of ~60 nm. Inset shows a scanning electron microscopy cross-section of such a ~60 nm channel. Scale bar: 200 nm.



Supplementary Fig. 23 | Threshold voltage (V_T) variability of all flexible MoS₂ FETs. V_T extracted with the linear extrapolation method. Most data are for EOT \sim 16.4 nm and some data for EOT \sim 13.7 nm (black). The different colors indicate separate growth and fabrication runs. We measured \sim 100 *Type A* and *Type B* devices, and the geometry, process flows or channel length did not discernably correlate with any V_T changes.

In the linear transistor operating region (at small V_{DS}), R_{ch} can be approximated as

$$R_{ch} = \frac{V_{DS}}{I_D} W \approx \frac{L}{\mu_{FE} C_{ox} (V_{GS} - V_T)},$$

where I_D , L , μ_{FE} , C_{ox} , V_{GS} and V_T are the drain current, channel length, intrinsic field-effect mobility, gate oxide capacitance per unit area, gate-source voltage and threshold voltage, respectively. Hence, taking into account R_{tot} when measuring the drain current ($I_{D,meas}$) while applying a voltage between drain and source ($V_{DS,appl}$), we obtain the following for $I_{D,meas}$ (normalized by W , unit: $A m^{-1}$):

$$I_{D,meas} = \frac{V_{DS,appl}}{R_{tot}} = \frac{V_{DS,appl}}{2R_C + \frac{L}{\mu_{FE} C_{ox} (V_{GS} - V_T)}}.$$

Thus, we have an expression for $I_{D,meas}$ where the denominator has two competing components which limit the maximum $I_{D,meas}$ that can be obtained. Further, we can find that for ultra-scaled transistors in the limit $L \rightarrow 0$, the maximum $I_{D,meas}$ is fully limited by R_C . In contrast, at long channel devices (here, $L \geq 10 \mu m$) the R_C no longer has significant impact and $I_{D,meas}$ is mainly defined by μ_{FE} , given the electrostatics and carrier concentration are fixed (C_{ox} , V_{GS} and V_T constant).

In the following, we use this model to identify lower and upper bounds for R_C and μ_{FE} based on our experimentally obtained results in flexible MoS₂ FETs with channel lengths ranging from \sim 10 μm down to \sim 60 nm. For that we extract $I_{D,meas}$ at $V_{DS} = 0.1$ V (Fig. 3d) at an overdrive gate voltage ($V_{ov} = V_{GS} - V_T = 8$ V) using a V_T extracted from a linear fit of g_m vs V_{GS} . In addition, our model needs C_{ox} , which in this case is $0.21 \mu F cm^{-2}$ or EOT \sim 16.4 nm (Supplementary Fig. 12a). With that, we can use

R_C and μ_{FE} as fitting parameters. We obtain upper bounds for $R_C = 2.3 \text{ k}\Omega \mu\text{m}$ and $\mu_{FE} = 27 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ for *Type B* devices. Taking into account also the best *Type A* devices, the upper bounds become $R_C = 0.25 \text{ k}\Omega \mu\text{m}$ and $\mu_{FE} = 30 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ indicating a remarkably reduced R_C for the *Type A* device at $L \sim 82 \text{ nm}$. Furthermore, it becomes evident that at channel lengths of $\sim 10 \mu\text{m}$ the devices are dominated by μ_{FE} as changes in R_C do not significantly impact I_D (dotted blue and solid black lines converge in Fig. 3d). This gives us the opportunity to fix the μ_{FE} range at $L \sim 10 \mu\text{m}$ and then subsequently fit R_C to the highest data points at the smallest channel lengths, where R_C has a larger impact than μ_{FE} , which gives us an estimate for the best R_C . We performed the fitting at $V_{DS} = 0.1 \text{ V}$ (Fig. 3d) to ensure that the devices are in the linear operating regime. We show in Fig. 3c,f that the devices with the highest I_D display effects of self-heating and velocity saturation even below V_{DS} values that would warrant channel pinch-off, which can be commonly observed for sub-100 nm channel length in MoS₂ FETs.^{7,39} However, this does not impact our model because we only use it at low V_{DS} . The model can also be used to predict the extrinsic field-effect mobility $\mu_{FE,ext}$. The above equations can be modified to:⁴⁰

$$\mu_{FE,ext} = \frac{\mu_{FE}}{1 + \frac{\mu_{FE} C_{ox} (V_{GS} - V_T)^2 R_C}{L}}$$

We used the same input parameters (R_C and μ_{FE}) for $\mu_{FE,ext}$ as for our I_D fitting. The result shown in Fig. 3e agrees with our extracted $\mu_{FE,ext}$ based on the maximum g_m method, confirming our calculations.

15. Correction for Lateral Current Spreading in *Type A* FETs

In all our TMD FETs of *Type A*, where the semiconductor width is greater than the electrode width, fringe currents can contribute non-negligibly to the total measured current depending on a number of factors including contact width and spacing, contact resistance and semiconductor mobility. In order to provide an accurate extraction and comparison of I_D and $\mu_{FE,ext}$ for *Type A* devices and estimate the fringe current effects, we define a dimensionless correction factor:

$$CF = \frac{I_D}{W I_{D,1D}}$$

where I_D is the total current (in μA), W is width of the contact and semiconductor overlap, and $I_{D,1D}$ is the width-normalized current (in $\mu\text{A} \mu\text{m}^{-1}$) in a FET with the same electrical parameters (sheet and contact resistances) but a channel geometry without current spreading. For FETs without a well-defined patterned channel, $CF > 1$, reflecting the contribution of fringe currents. In the linear regime of the transistor, given R_C , μ_{FE} and bias voltages; $I_{D,1D}$ can be calculated as $V_{DS} \cdot W^{-1} \cdot R_{tot}^{-1}$, with R_{tot}

calculated as defined in the previous section. I_D depends on the device and contact geometry as well: we estimate it using 2D finite element method (FEM) simulations using COMSOL Multiphysics to calculate the current distribution. With CF so obtained, width-normalized corrected currents are then

$$I_{D,corr} = \frac{1}{CF} \frac{I_{D,meas}}{W}.$$

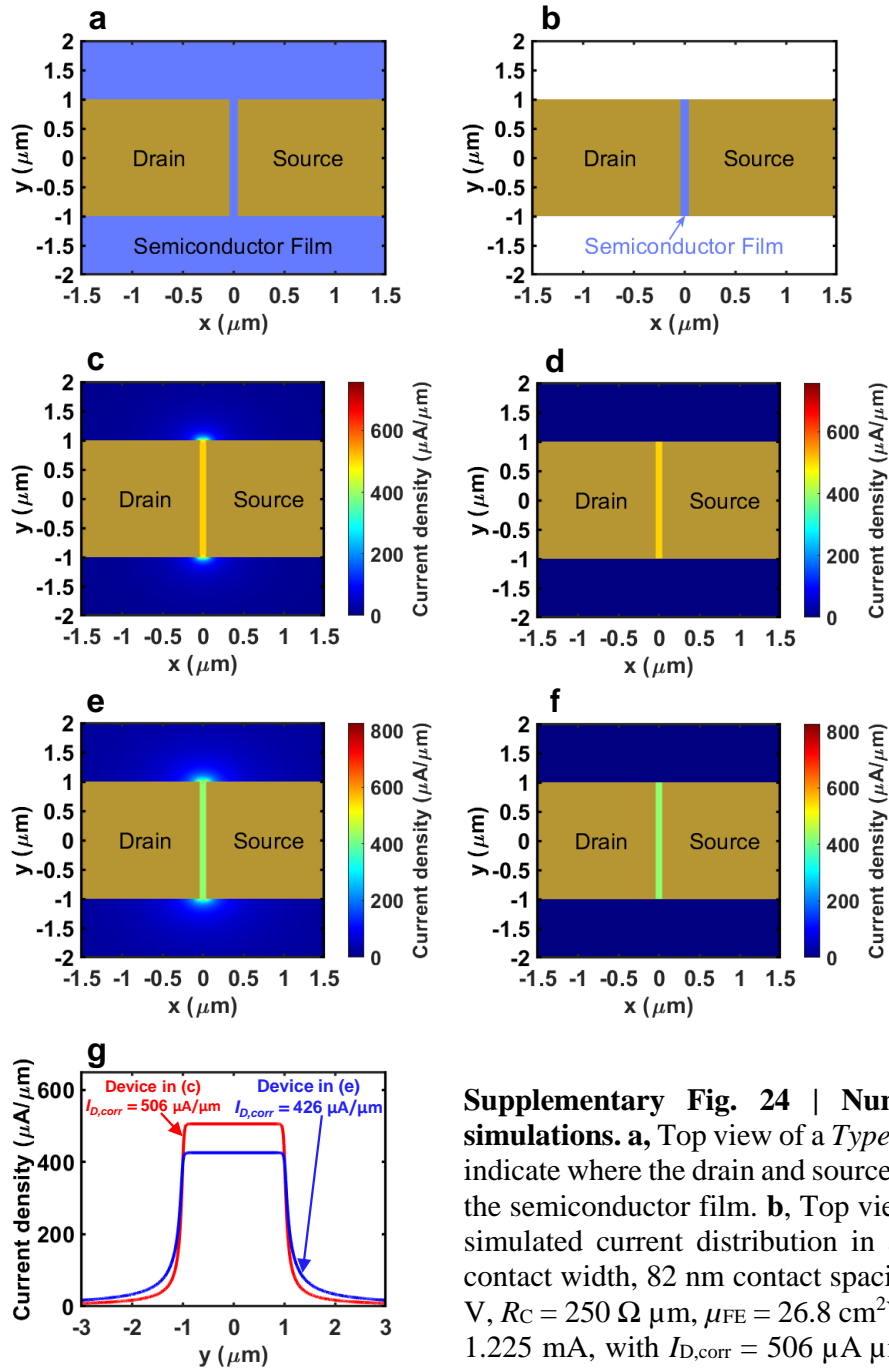
In FEM simulations, the transistor is assumed to be in the linear region of operation with $V_{DS} \ll V_{GS} - V_T$, so the semiconductor sheet resistance is assumed to be the same everywhere (except where the semiconductor overlaps with contacts), and given by

$$R_{sh} = \frac{1}{\mu_{FE} C_{ox} (V_{GS} - V_T)}.$$

For purposes of calculating this current distribution, the contacts are assumed to be edge contacts¹⁰⁰ with a contact resistance per unit width of R_C . The edge contact assumption is equivalent to contacts with current transfer length²⁴ $L_T < 50$ nm.

The two unknown electrical parameters that influence CF are μ_{FE} and R_C . However, for devices without a patterned channel, it is not straightforward to extract these directly from electrical data while simultaneously correcting for fringe currents: a range of CF are possible for different combinations of μ_{FE} and R_C . For the lower end of this range, we assume an $R_C = 250 \Omega \mu\text{m}$ (best prior reported results for CVD MoS₂ with Au contacts),²⁸ and fit μ_{FE} to get the measured I_D . For the upper CF estimate, we assume μ_{FE} about 2-fold higher than in our best devices (for CVD MoS₂ a similar value to best prior results on silicon)²⁸ resulting in $\mu_{FE} = 56 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ for MoS₂, $5 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ for MoSe₂ and $10 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ for WSe₂, then fit R_C to get the measured I_D . The range of CF calculated this way yields a range of $I_{D,corr}$ and $\mu_{FE,ext}$, which is illustrated as vertical bars in e.g., Figs. 3d and 3e.

An example for the current spreading correction is displayed in Supplementary Fig. 24 for an 82 nm long MoS₂ FET. The FEM simulation result displays the current flow paths for two different scenarios of fitted R_C/μ_{FE} (Supplementary Figs. 24c,e). It is visible that the spreading is more pronounced for the scenario with higher μ_{FE} and higher R_C . In Supplementary Figs. 24d and f, the respective I_D distributions with a hypothetical channel width = electrode width are shown which yield $I_{D,ID}$. For this device, we reported in the main manuscript the average values for these two bounds, which is $\sim 466 \mu\text{A} \mu\text{m}^{-1}$. Finally, Supplementary Fig. 24g displays the current distribution in the y-direction (perpendicular to the channel) at the channel center (defined as $x = 0$), which visualizes the current spreading effect for the two different fitting scenarios.



Supplementary Fig. 24 | Numerical current spreading simulations.

a, Top view of a *Type A* device. The regions in gold indicate where the drain and source electrodes are in contact with the semiconductor film. **b**, Top view of a *Type B* device. **c**, The simulated current distribution in a *Type A* device with 2 μm contact width, 82 nm contact spacing, $V_{GS} - V_T = 10$ V, $V_{DS} = 1$ V, $R_C = 250 \Omega \mu\text{m}$, $\mu_{FE} = 26.8 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$. The resulting current is 1.225 mA, with $I_{D,\text{corr}} = 506 \mu\text{A} \mu\text{m}^{-1}$ ($CF = 1.211$). This set of R_C and μ_{FE} yields the upper bound of our estimated range of $I_{D,\text{corr}}$

values. **d**, The current distribution in the corresponding *Type B* device with the same electrical parameters as in c. The width-normalized current is equal to $I_{D,\text{corr}} = 506 \mu\text{A} \mu\text{m}^{-1}$. **e**, The simulated current distribution in a *Type A* device with 2 μm contact width, at the same bias conditions as in c but with $R_C = 821 \Omega \mu\text{m}$, $\mu_{FE} = 56 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$. The resulting current is also 1.225 mA, with $I_{D,\text{corr}} = 426 \mu\text{A} \mu\text{m}^{-1}$ ($CF = 1.438$). This set of R_C and μ_{FE} yields the lower bound of our estimated range of $I_{D,\text{corr}}$ values. **f**, The current distribution in the corresponding *Type B* device with the same electrical parameters as in e. The width-normalized current is equal to $I_{D,\text{corr}} = 426 \mu\text{A} \mu\text{m}^{-1}$. **g**, The current density midway between the contacts ($x = 0$) as a function of the y -coordinate. Red and blue curves correspond to the *Type A* devices c and e, respectively.

16. Benchmarking Tables

Reference	Synthesis method	Thickness (nm)	Length (nm)	μ_{FE} or $\mu_{FE,ext}$ ($\text{cm}^2\text{V}^{-1}\text{s}^{-1}$)	I_D at $V_{DS} = 1\text{V}$ ($\mu\text{A}\mu\text{m}^{-1}$)
Kwon et al. ⁴⁴	exfoliated	30-80	7000	44.8	4.1
Chang et al. ⁴⁵	exfoliated	7.9	1000	30*	13
Yoon et al. ⁴⁶	exfoliated	3.075 (5 layers)	4000	4.7	0.3
Lee et al. ⁴⁷	exfoliated	1.845 (3 layers)	800	29	NA
Salvatore et al. ⁴	exfoliated	3.5	4300	19	1.3
Yoo et al. ⁴⁸	exfoliated	66.5	8300	83.5	3
Song et al. ⁴⁹	exfoliated	79.3	22600	141.3	1.2
Cheng et al. ¹⁶	exfoliated	1.845 (3 layers)	116	NA	48**
Cheng et al. ¹⁶	exfoliated	1.845 (3 layers)	68	NA	135***
Ma et al. ⁵⁰	exfoliated	18.3	17500	15.5 ± 15.9	0.32
Chang et al. ¹⁷	CVD	0.615 (1 layer)	750	31*	66
Amani et al. ⁵¹	CVD	0.615 (1 layer)	13000	18.9*	0.2
Shinde et al. ³²	CVD	0.615 (1 layer)	4000	6.7 ± 20	2.2
Woo et al. ⁵²	CVD	1.538 (2.5 layers)	10000	9	1.4
Park et al. ⁵³	CVD	1.23 (2 layers)	4000	17.4	0.13

Supplementary Table 2: Literature values for flexible MoS₂ field-effect transistors used to generate Figs. 4a,b. The synthesis method denotes whether the material was mechanically exfoliated or grown by chemical vapor deposition (CVD). * indicates that in these cases the field-effect mobility μ_{FE} was extracted by the y-function method and contact resistance R_C is excluded. For the other cases the method was either not specified or the transconductance g_m maximum method was used which results in an extrinsic μ_{FE} ($\mu_{FE,ext}$). The drain current I_D is in most cases specified at a drain-source voltage $V_{DS} = 1\text{V}$, unless labeled: ** $V_{DS} = 2\text{V}$, *** V_{DS} not specified.

Reference	Channel material	Length (nm)	on/off ratio	I_D at $V_{DS} = 0.5\text{V}$ ($\mu\text{A}\mu\text{m}^{-1}$)
Park et al. ⁵⁵	graphene	140	1.5	248
Yeh et al. ⁵⁶	graphene	200	8.8	516
Zhai et al. ⁵⁴	single-crystal silicon (c-Si)	150	6×10^7	369
Shahrjerdi et al. ⁴³	single-crystal silicon (c-Si)	30	2×10^5	714
Wang et al. ⁵⁷	InSnO (ITO)	160	7×10^8	34
Münzenrieder et al. ⁵⁸	InGaZnO (IGZO)	160	7.1	119
Cheng et al. ¹⁶	MoS ₂	116	2×10^6	48*
Cheng et al. ¹⁶	MoS ₂	68	10^6	135**

Supplementary Table 3: Literature values for flexible field-effect transistors with channel lengths $\leq 200\text{nm}$ used to generate Fig. 4c. The drain current I_D is in most cases specified at a drain-source voltage $V_{DS} = 0.5\text{V}$, unless labelled: * $V_{DS} = 2\text{V}$, ** V_{DS} not specified.

17. Estimation of the transit frequency

The scope of this work has been to demonstrate nanoscale flexible TMD transistors with high dc performance. The top gate, fabricated after release of the flexible substrate, is currently still limited by available process accuracy for alignment and feature size in the optical lithography on the ultra-thin flexible substrate. This leads to a large overlap area, and hence high overlap capacitance, which will

limit the ac device performance. The reduction of parasitic overlaps will be addressed in future work. Nevertheless, to evaluate the potential of our devices for high frequency applications, we calculated the expected transit frequency f_T of our transistors with highest performance. We have used the extracted $\mu_{FE,ext}$ at $V_{DS} = 1$ V, which lumps together material parameters (μ_{FE}) and other device parasitics (RC), and hence we can estimate f_T , based on the following equation (adapted from other works^{40,101}):

$$f_T = \frac{\mu_{FE,ext} V_{DS} C_{ox} W_{ch}}{2\pi L_{ch} C_{tot}}$$

where C_{tot} is the total capacitance and other variables were previously defined (see Supplementary Section 14). C_{tot} has several components: 1) the total gate oxide capacitance including overlaps ($C_{ox,tot}$), 2) the parasitic capacitance from the sidewall of the gate (C_{side}), and 3) the fringing parasitic capacitance from the top surface of the gate (C_{top}).

$$C_{tot} = C_{ox,tot} + 2(C_{side} + C_{top})$$

$C_{ox,tot}$, C_{side} and C_{top} are then estimated as follows:^{40,101,102}

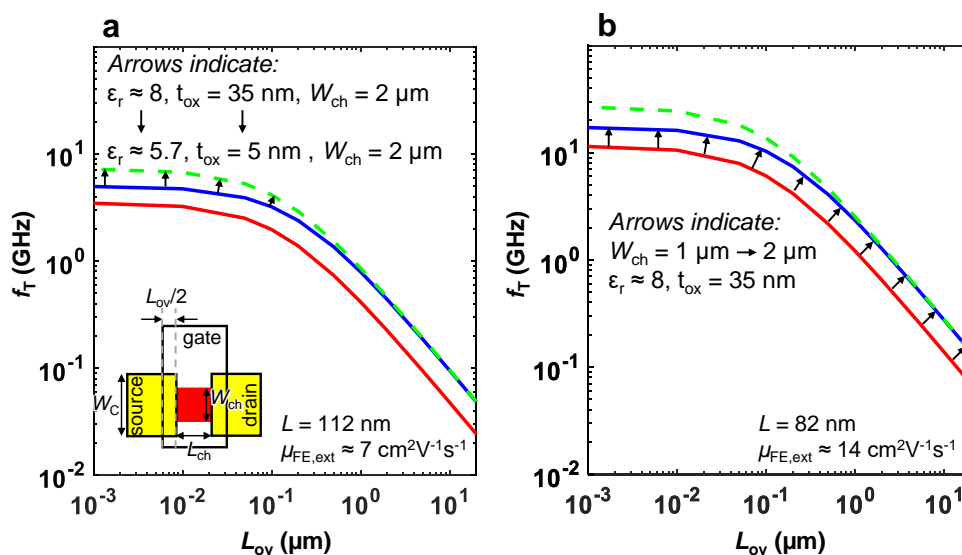
$$C_{ox,tot} = C_{ox}(L_{ch}W_{ch} + L_{ov}W_C)$$

$$C_{side} = \frac{W_C \varepsilon_0 \varepsilon_r}{\pi} \ln \left[(K^2 - 1) \left(\frac{K^2}{K^2 - 1} \right)^{K^2} \right]$$

$$C_{top} = \frac{W_C \varepsilon_0 \varepsilon_r}{\pi} \ln \left[1 + \frac{L_{ch} + L_{ov}}{t_{ox} + t_{gate}} \right]$$

where $K = 1 + t_{gate}/t_{ox}$ with t_{gate} as the gate metal thickness and t_{ox} as the gate oxide thickness, ε_0 as the vacuum permittivity, ε_r as the relative gate oxide permittivity, L_{ov} is the gate-source/drain overlap length (see inset of Supplementary Figure 25) and other variables were previously defined.

Thus we calculate f_T as a function of L_{ov} , which is displayed in Supplementary Figure 25 taking the corresponding dc data from the devices shown in Fig. 3c,f. Initially, we assumed similar device geometry as in our *Type B* devices with our measured $C_{ox} \approx 0.21 \mu\text{F cm}^{-2}$, $\varepsilon_r \approx 8$, $t_{ox} \approx 35$ nm (see Supplementary Section 5), $t_{gate} = 65$ nm, $W_{ch} = 1 \mu\text{m}$ and $W_C = 2 \mu\text{m}$. The inset sketches the different geometrical parameters in top view. The resulting f_T is displayed in red. We find a strong dependence on L_{ov} for large overlaps $> 0.1 \mu\text{m}$ where the parasitic overlap capacitance dominates. A general improvement in f_T can be expected when W_{ch} is increased to a value equal to W_C (blue lines, and arrows in Supplementary Figure 25b). In addition, decreasing the gate oxide thickness will only lead to higher f_T if gate-source/drain overlaps are minimized ($< 0.1 \mu\text{m}$, green dashed lines, and arrows in Supplementary Figure 25a). We have estimated here the case for reducing our Al_2O_3 gate dielectric thickness to 5 nm, which would lead to a lower ε_r due to interface effects and C_{ox} would become $\approx 1 \mu\text{F cm}^{-2}$.^{77,103} The maximum f_T estimated after these modifications reaches ~ 26 GHz, and could be increased slightly more by reducing t_{gate} which for instance would lead to ~ 27 GHz for $t_{gate} = 15$ nm.



Supplementary Fig. 25 | Calculated transit frequency f_T as a function of gate-to-source/drain overlap length L_{ov} . The calculation was done based on dc characteristics shown in **a**, Fig. 3c and **b**, Fig. 3f. The inset in **a** sketches the geometry used for the calculations.

These results indicate that the first priority should be minimizing L_{ov} which could be done by advanced lithography techniques or fabrication tricks (like self-alignment¹⁰⁴). However, it should be noted that an underlapped device structure, which avoids parasitic overlap capacitance overall could significantly increase the access resistance (and R_C)¹⁷ without a stable and reliable TMD doping technology. Thus, a careful optimization of the device geometry will be necessary. Nevertheless, our estimation of maximum f_T of ~ 7 GHz and ~ 27 GHz for the two selected devices demonstrate the potential of high frequency operation in flexible MoS₂ transistors.

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