Enhancing Hysteresis in Graphene Devices Using Dielectric Screening

Kevin Brenner, T. J. Beck, and James D. Meindl, *Life Fellow, IEEE*

***Abstract*—A method of increasing hysteresis in graphene devices with a dielectric coating is presented. By controlling the sweep direction of the gate bias, "high-conductance" and "low-conductance" states can be produced by transitioning the device between dielectric screened and unscreened states, which is a fundamentally new approach to producing hysteresis. Moderate carrier densities ($\sim 4 \times 10^{12}$ cm^{-2}) result in field-driven injection of charge from the graphene channel into the underlying SiO_2 substrate, modifying the scattering charged-impurity layout seen by the graphene, ultimately disrupting the steady-state screening process. A stable room-temperature conductance gap of nearly one order of magnitude is demonstrated.**

***Index Terms*—Charged-impurity scattering, dielectric screening, graphene, graphene devices, hysteresis, memory.**

I. Introduction

ATOMICALLY thin carbon devices are highly attractive for sensor applications, owing to their heightened dependence of bulk conductance to adsorbates and charges in the vicinity of the channel [1]. Historically, the ability of such devices to *sense* relied on a modification of the carrier density by the external species, which trickles into a measurable deviation in conductance [2]. Memory applications are perfect niches for such carbon devices, where a drive for operation based on single-electron sensitivity exists [3], [4]. Thus far, the most promising memory devices in carbon nanotubes (CNTs) and graphene nanoribbons (GNRs) have taken the form of floating-gate architectures, where hysteresis from the screening of locally pinned charge results in a shift in carrier density and, ultimately, a displacement of the threshold voltage [4]. However, such devices require a bandgap and are limited to low-temperature operation [2], with gapped GNRs being additionally plagued by vast reductions in mobility [5]. New routes for producing hysteresis and enhancing the sensitivity of quasi-2-D systems are expected to have a far-reaching impact for carbon devices [6].

In this letter, we present a fundamentally new approach to producing hysteresis in graphene devices. Field-driven injection of charge into the underlying SiO_2 substrate is used to modify the layout of charged-impurity scatterers seen by the graphene channel. By coating the device with the dielectric material dimethylformamide (DMF), "low-conductance" and "high-conductance" states are observed by disrupting and reinstating the dielectric screening process. Here, external species modify the conductance through their role as scatterers rather than dopants. This paradigm shift in the sensing mechanism is expected to excite new avenues for ultrahigh sensitivity in carbon devices. Atomically thin carbon devices offer the possibility of designing nanoscale ballistic systems that become diffusive by the addition of a single scattering charge.

II. Experiment

Devices are fabricated using mechanically exfoliated graphene applied to a Si substrate with 300 nm of thermally grown oxide [7]. The application of graphene occurs while the substrate is at an elevated temperature (> 200 °C) to fully desorb bound water molecules [8], allowing for an intimate contact. The graphene flakes on scotch tape are loaded into a standard glovebox that maintains a dry N_2 environment. The substrate is prepared using a solvent rinse and a 10-s exposure to a low-power oxygen plasma to remove organic residues. The substrate is loaded within the same glovebox and placed on a hot plate at 300 °C to bake for 24 h. The graphene is applied via gentle pressure to the scotch tape in contact with the hot substrate surface. The substrate is then removed from the hot plate/glovebox for further processing. Monolayer graphene is identified by optical contrast and verified using atomic force microscopy (AFM) [9] and Raman spectroscopy. Contact metallization is patterned using electron-beam lithography, followed by evaporation of a Ti/Au (10 nm/80 nm) stack. A total of 15 devices were fabricated. The channel length is defined by the inner contacts and is pinned at 3 μm to avoid doping effects from the metallization. The channel width is defined by the exfoliation. The device is pumped for 24 h at a vacuum of 1.5×10^{-6} torr to remove atmospheric adsorbates. When drop casting is performed, the vacuum is broken, and a loop of the back-gate bias is continually pulsed using hold and off times of 1 and 15 ms, respectively. Four-point electrical testing at a 50-mV drain–source bias is used to remove contact resistance (r_c) from our measurements. However, r_c was extracted by comparing the four-point to two-point measurements and found to be $\sim 30\ \Omega$, which is over an order of magnitude below our channel resistance. Four-point testing and a pulsed back gate are used for all measurements in this letter.

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The authors are with the Nanoelectronics Research Center, Georgia Institute of Technology, Atlanta, GA 30332 USA (e-mail: kevin.brenner@gatech.edu).

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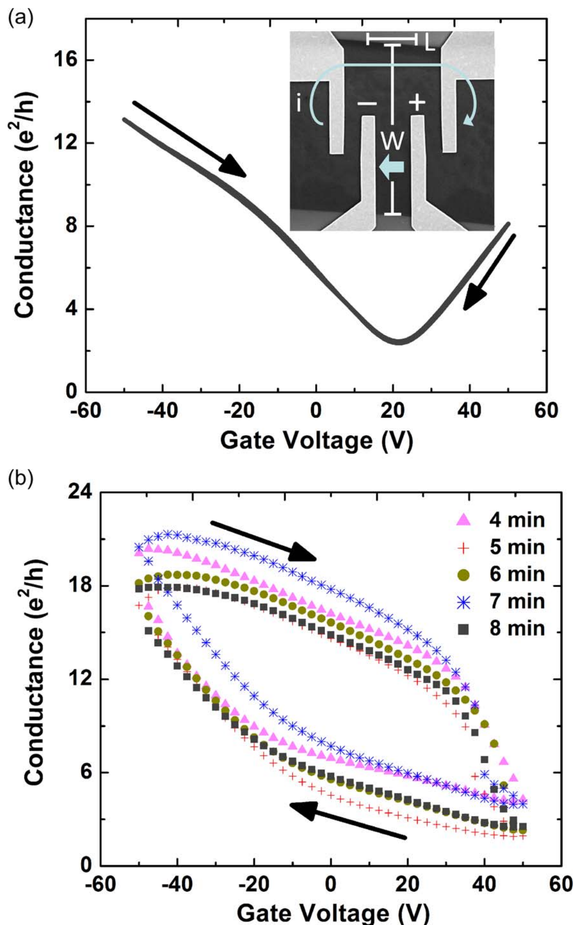

Fig. 1. Demonstration of a stable room-temperature hysteresis. (a) Pristine graphene, prior to drop casting, shows no signs of a significant hysteresis. The inset shows an annotated SEM image of the device, indicating the four-point setup. (b) After DMF coating, a stable hysteresis of nearly one order of magnitude is observed at room temperature.

III. Results and Discussion

Electrical testing of a single device is shown in Fig. 1. The pristine device is exposed to the ambient environment and exhibits no observable hysteresis [Fig. 1(a)]. After 30 s of ambient exposure, a 10-μL film of DMF is drop cast using a microsyringe. A 3-min break-in time is attributed to mechanical settling of the probe tips which could be disturbed during the drop casting, as well as the formation of a significant trap population below the channel. A stable room-temperature conductance gap of nearly one order of magnitude ($2-20\,e^2/h$) is demonstrated, where e is the elementary charge and h is Planck's constant [Fig. 1(b)]. The low-conductance state on the forward sweep is on par with the pristine unscreened conductance state observed in Fig. 1(a). The high-conductance screened state agrees with the previous values for DMF coating of graphene [10], confirming that the hysteresis results from a turning-on and a turning-off of the dielectric screening process. The values presented in [8] were internally verified on a batch of devices in our setup. After 8 min, the hysteresis becomes unstable due to evaporation of the DMF.

Mobility in graphene devices is severely limited by charged impurities in the vicinity of the channel [11], resulting in significant reductions in conductance. Coating graphene with a dielectric has been shown to be capable of screening charged impurities. Over one order of magnitude improvement in conductance with proper selection of the dielectric and a heavily scattered channel is possible [12], [13]. There are two fundamental mechanisms that drive hysteresis in carbon devices supported by SiO_2. The first is charge trapping of adsorbed water vapor and hydroxyl groups on or in proximity to the carbon channel [14]. The second mechanism involves field-driven emission of charge from the carbon channel into the underlying substrate [4], [15]. The millisecond back-gate pulse times used in this work occur on a time scale more rapid than the charge-trapping time associated with atmospheric adsorbates, which are on the order of 0.1–10 s [16], making charge injection from the graphene the primary driver of hysteresis. Modeling of the injection of electrons from CNTs into the underlying oxide has been previously carried out [15], [17]. The injection and release of electrons locally embedded in the SiO_2 are functions of the electric field ($E_{\rm int}$) at the channel/oxide interface. The magnitude of $E_{\rm int}$ is a function of the external potential, which is dominated by the carrier density (n) in the graphene device. The back-gate voltage is tied to n through the following expression: $C_{\rm ox} \cdot (V_g - V_0) = e \cdot n$. Here, $C_{\rm ox}$ for 300 nm is 11.6 nF/cm^2, and $V_g - V_0$ is the displacement of the minimum conductivity point (i.e., where the Fermi level is pinned in the vicinity of the Dirac point) from zero gate bias. Carrier densities beyond 2×10^{12} cm^{-2} should exist in the graphene sheet at the extremes of the gate voltage loop. Based on our AFM measurements, the graphene sheet is taken as a 3.5-Å-thick uniform plane of charge [9]. An intimate contact with the substrate, which is oxide coated with a single layer of silanol groups, is assumed given the elevated temperature of the substrate during exfoliation [8], [18], producing an interfacial spacing of approximately 1 Å ($d_{\rm int}$). The magnitude of the electric field resulting from the charge in the graphene channel can be expressed using the Poisson equation

$$E_{\rm int} = \frac{qn}{\varepsilon} d_{\rm int}. \tag{1}$$

This results in electric fields at the interface on the order of 0.2 V/nm, which is comparable to the breakdown field for SiO_2 [4], [19], facilitating the local embedding and release of electrons directly from the channel.

Injected electrons into the oxide reside close the carbon/SiO_2 interface at depths on the order of 3 nm [15]–[17]. The Thomas–Fermi screening length (λ) for graphene is defined as $\lambda = 1/(4k_F\alpha)$, where $k_F = (\pi n)^{1/2}$ and $\alpha = 2e^2/hv_f(K_1 + K_2)$ [13]. For this specific system, K_1 is the dielectric constant of SiO_2, and K_2 is the dielectric constant of DMF, which are $\sim$3.9 and $\sim$36, respectively. Assuming a carrier concentration of $n = 1 \times 10^{12}$ cm^{-2}, the screening length for injected charged is over 25 nm. Since the charge from the graphene is injected at narrow depths, even multilayer graphene systems are not sufficient to effectively screen trapped oxide charge, resulting in a residual electric field penetrating into the DMF film. An explanation of the hysteresis mechanism is shown in Fig. 2. At large positive values of the gate bias, electrons are emitted from the graphene and embedded into the underlying oxide, producing a new scattering layout of negatively charged

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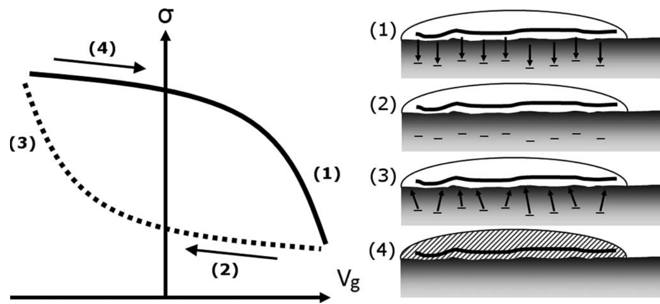

Fig. 2. Illustration of the hysteresis mechanism. (1) Injected charge from the graphene channel degrades (2) conductance on the leftward sweep. This low-conductance state remains until the charge is released at (3) large negative gate voltages, resulting in (4) a return to high conductance on the rightward sweep.

impurities. The result of these scatterers is a low-conductance (unscreened) state observed on the leftward sweep of the gate bias. These scatterers are eventually released at large negative values of the gate voltage, ushering a return to the high-conductance (screened) state seen on the rightward sweep of the gate bias.

From a scalability standpoint, the operating voltage required for charge injection, i.e., switching, can be vastly reduced by thinning the gate dielectric beyond 300 nm. In terms of the conductance gap, atomically thin carbon devices (CNT and GNRs) offer an entirely unique platform for ballistic transport across micrometer lengths. The ultimate limit for devices leveraging single-electron sensitivity is first envisioned here, where the transition between ballistic and diffusive transport can occur in graphene channels from the self-emission of a lone charged scatterer.

IV. Conclusion

A graphene device exhibiting a room-temperature conductance hysteresis of nearly one order of magnitude has been demonstrated. It is shown that, by coating graphene with a dielectric, a transition from a screened "high-conductance" state to an unscreened "low-conductance" state can be produced. The disruption and reinstating of the steady-state screening process is found to be driven by charge injection from the graphene channel. This letter has presented the first demonstration of a potential floating-gate device where external charge is utilized as a scattering mechanism to modify conductance, which is a new approach to enhancing the sensitivity of atomically thin carbon devices.

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