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Ultra-High Mobility in Dielectrically Pinned CVD Graphene

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ABSTRACT We report improved control over the quality and uniformity of CVD graphene devices through a novel fabrication technique. An overlying HSQ pinning dielectric is used to physically anchor and protect the graphene sheet, resulting in electron and hole motilities of 25 600 and 23 700 cm^2/Vs, respectively, record-breaking values for CVD graphene devices. Transitioning from traditional 3-D bulk materials to loosely adhered 2-D graphene sheets, the presented process is expected to bring new focus to post-transfer passivation as a means of fabricating graphene devices closer to their theoretical limits. Based on the extracted mean-free-path (MFP) from the experimental data, the graphene interconnect is benchmarked against the copper interconnect at various widths and edge roughness. Results demonstrate the importance of edge smoothness and MFP, which dictate the potential benefits of graphene interconnects at a narrow dimension.

INDEX TERMS CVD graphene, dielectric screening, electron mobility, energy-delay product, interconnects, mean-free-path.

I. INTRODUCTION

Physical scaling of the complimentary metal-oxide-semiconductor (CMOS) minimum feature size has been a driving force behind the semiconductor industry for over half a century. Specifically, selection of a process technology can dictate both the cost and performance of a chipset. Historically, the performance of a chipset was dominated by the performance of transistors [1]. However, as the feature size shrinks below 100nm, interconnects become the dominating factor in determining performance [2]. This interconnect-limited performance stems from the increasing resistance of the interconnect material, copper (Cu), with scaling. This effect is intrinsic to various sidewall and grain-boundary scattering mechanisms in the Cu itself and is difficult to overcome through design changes [3]. As such, the semiconductor industry is actively seeking replacement materials to Cu to enable future CMOS scaling.

Graphene is considered a promising novel interconnect material owing to its intrinsic electrical properties. These include an impressive current carrying capability (10^8 A/cm^2) [4], high intrinsic mobility (200,000 cm^2/Vs) [5], and low capacitance [6]. To date, most of these properties are washed out by fabrication-induced damage, making real-life graphene devices a poor reflection of their theoretical benchmarks. In transitioning from traditional three-dimensional (3D) bulk materials to loosely adhered 2D graphene sheets, electrical properties can be lost in process steps that are commonplace to CMOS fabrication. We have observed that the possible roadblocks to graphene adoption within a commercial CMOS line are not all tied to the synthesis or even transfer process steps, but to fabrication damage post-transfer. Processing steps such as the stripping of multiple soft masks, spin/spray coating, and aqueous soaks induce tears, folds, and ultimately defects that cripple mobility and place device-to-device variability outside any acceptable commercial envelope.

Most recent fabrication advancements have focused on either the synthesis or transfer process steps for chemical vapor deposition (CVD) graphene [7]. CVD graphene is widely regarded as the most promising synthesis technique

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for large-scale integration. Specifically, pristine and uniform CVD graphene can be produced on Cu templates capable of supporting 200-300mm wafers [8]. Moreover, various transfer methods have been proposed to remove graphene sheets from their high-temperature synthesis template and apply them to a target wafer within the thermal budget of mainstream CMOS [7]. While both the quality of as-grown and as-transferred CVD graphene can be high, fabricated CVD graphene devices tend to exhibit relatively poor mobility in the range of 200-4000 cm^2/Vs [9]–[13]. These mobilities reflect only 10% of the theoretical phonon-limited mobility of graphene on a dielectric (40,000 cm^2/Vs) [14].

In this work, we present a simple approach to fabricate high mobility CVD graphene devices with a record-breaking mobility of 25,600 cm^2/Vs and near perfect symmetry between the n- and p-branches. The approach is based on using hydrogen silsesquioxane (HSQ) as a dielectric to immediately pin down the CVD graphene sheet, post-transfer. This pinning dielectric provides a two-fold benefit: (1) mechanically anchors and protects the graphene and (2) provides a screening medium for charged impurities. In securing the graphene, peripheral issues related to the poor adhesion of contact metals to the graphene surface and mechanical abrasion at the graphene-SiO_2 interface during agitation are addressed.

The rest of the paper is organized as follows. Section II describes the fabrication process of the graphene devices. In Section III, we discuss the electrical performance of the fabricated devices based on four-probe measurements as well as Raman spectroscopy. Section IV illustrates the effect of various etchants on HSQ etch rate. Section V examines the feasibility of graphene interconnects for future IC technology nodes based on the ITRS roadmap. Finally, the Conclusion is given in Section VI.

II. FABRICATION PROCESS

Our fabrication process flow is summarized in Fig. 1a. The starting material is a 3cm × 3cm monolayer CVD graphene sheet atop 300nm of SiO_2 via a wet transfer process from ACS Materials. A 40nm film of 2% Hydrogen Silsesquioxane (HSQ) is spin-coated at 2000rpm for 60s with a ramp of 1000rpm/s. A JEOL JBX-9300FS Electron-Beam Lithography (EBL) System with a current of 2nA and a voltage of 100kV was used to pattern 10μm × 30μm rectangles. During exposure, the HSQ forms a thin dielectric layer of dense, network-like, SiO_2 atop the graphene. The sample was then developed in MF-319 for 70s followed by 9:1 DI:MF-319 for 1min and then DI water for 1 min. The sample is then dried with a light flow of N_2. Next, the HSQ pattern is transferred into the graphene layer using (Ar) plasma etch. Argon is used to avoid unintentional graphene doping from plasma species [15]. Whereas a normal process flow would strip the HSQ etch mask to apply metal contacts, we leave the HSQ as a dielectric to pin down the graphene and open via to make metal contacts. A second EBL step, aligned to the HSQ, patterns both the via and metal pads. A 500nm film of ZEP520A resist was spin-coated at 2000rpm for 60s with a ramp of 1000rpm/s. The pattern was exposed with a dose of 500$\mu C/cm^2$, followed by development in Amyl Acetate for 120s and an IPA rinse with N_2 drying. Via to the graphene surface are opened using the wet chemical etch described below. Finally, Ti/Au metal contacts (20/80nm) are deposited by Electron-Beam Evaporation followed by a standard liftoff procedure in 1165 at 120°C for 24hrs.

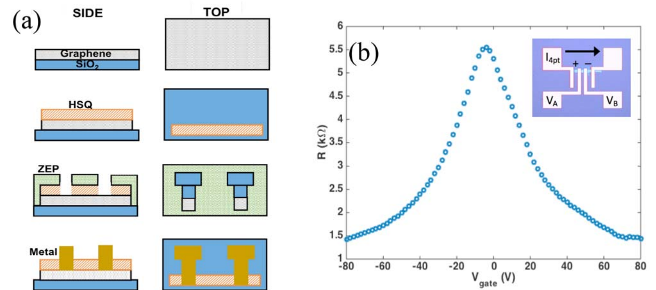

FIGURE 1. **(a) The general process flow for a dielectrically pinned CVD graphene. First, the starting material is CVD graphene on SiO_2. Next, EBL is used to pattern the graphene with HSQ. Next, the HSQ pattern is transferred into the graphene via a plasma etch. Next, a second EBL layer with ZEP is used to pattern via and contact pads. Next, the vias are opened by clearing the HSQ using a wet etch. Next, contact metal is deposited using E-Beam. Finally, the excess metal is removed using a standard liftoff procedure, (b) Transfer characteristics from four-point measurements on a typical pinned CVD graphene device. An optical image of the device is shown in the inset. Four-point testing is performed by passing an excitation current around the outer pads and measuring the voltage drop across the inner pads.**

III. ELECTRICAL PERFORMANCE

The transfer characteristics of a typical device are shown above in Fig. 1b. Electrical testing is performed under vacuum (1×10^{-3} Torr for 24hrs) in a Lakeshore probe station at room temperature. A Keithley 2612a source meter is used in a four-point configuration to remove any contact resistance from the readings. A pulsed back-gate technique is also used to remove potential hysteresis from charge trapping [16]. Mobility is extracted at a residual carrier concentration of 1.43×10^{11} cm^{-2}. The relation between the gate voltage and carrier density is determined through the expression:

$$C_{OX} \cdot \left(V_g - V_{\min}\right) = n \ . \ q, \tag{1}$$

where V_g is the applied back-gate voltage, V_{min} is position of the minimum conductivity point, n is the carrier density, q is the elementary charge (1.602×10^{-19} C), and C_{ox} is the oxide capacitance (11.6nF/cm^2 for the 300nm SiO_2 dielectric used in this work). The gated curve of Fig. 1b yields record-breaking electron and hole mobilities of 25,600 and 23,700 cm^2/Vs, respectively, for the 10 × 30 μm device. This is a 60% improvement compared to the highest mobility for CVD graphene recorded to date on SiO_2 substrate [17]. Furthermore, this value is only 36% away from the theoretical mobility limit of graphene on SiO_2 predicted by

Chen *et al.* [18]. The measurements also show that electron and hole mobilities are highly symmetric and the Dirac point is very close to zero (−4V), which signifies a minimal unintentional doping from oxygen and water molecules.

The high quality of these devices is attributed to the presence of the HSQ for two main reasons. First and foremost, HSQ acts as a screening layer for the charged impurities located in the SiO_2 substrate. The Fourier transform of the potential of a charged impurity is given by [19]:

$$V_i^0(q) = \frac{2\pi e^2}{\kappa q} \tag{2}$$

where κ is proportional to the screening (dielectric) constant, which is the average dielectric constant of the material below and above the graphene sheet. In the absence of HSQ, the average dielectric constant is given by averaging the dielectric constant of SiO_2 ($\kappa_{siO_2} = 3.9$) and that of air ($\kappa_{air} = 1$); that is $\kappa_{avg} = (3.9 + 1)/2 \approx 2.5$. Adding HSQ ($\kappa_{HSQ} = 4$) increases the average dielectric constant to ~4. From equation (2), the potential created by the charge impurities is reduced and hence the force felt by an electron flowing across the graphene interconnect is reduced, which in turn minimizes scattering. Earlier reports have shown that high-k mediums atop graphene lead to a sharp R-V_g curve; hence improving mobility [20]. Furthermore, the screening of charged impurities also eliminates the asymmetry between electron and hole mobilities since this asymmetry was shown to originate from the different scattering cross sections for electrons and holes by the charged impurities [21].

Secondly, HSQ acts as a pinning dielectric. This overlying dielectric mechanically anchors and protects the graphene sheet from process damage. Moreover, the relatively weak adhesion between graphene and SiO_2 (~0.2 J/m^2) [22] opens avenues for shifting and abrasion at the graphene-SiO_2 interface during mechanically aggressive process steps [22]; specifically, spin/spray coating, aqueous soaks, and depositions. Pinning down graphene to the substrate allows for an accurate patterning of structures. It also improves the back gate control of graphene and enhances its contact resistance. Fig. 2 compares a device array that followed a non-pinned process flow (same synthesis and transfer process) with a device array fabricated using HSQ pinning. For the unpinned devices, metal contacts (Ti/Au) are patterned directly onto the CVD graphene sheet using EBL with ZEP520A. Despite good adhesion between the Ti and graphene surface, the metal pattern provides and optical indicator of the degree of graphene sheering from the SiO_2 surface. It is worth mentioning that HSQ specifically provides a very appealing material to be used as a top layer on graphene for the following reasons: (1) it saves extra fabrication steps by being an e-beam pattern for the graphene devices as well as providing dielectric screening and mechanical anchoring, (2) it is deposited on graphene by spin-coating which introduces the least number of defects to graphene compared to other methods such as e-beam evaporation and RF sputtering [23], and (3) due to the high tunability of its dielectric constant based on the degree of cross-linking [24].

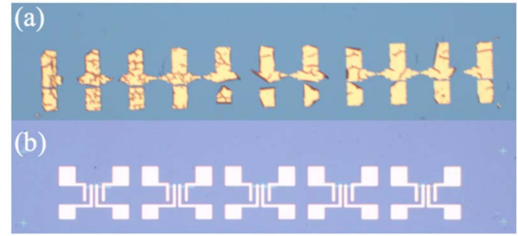

FIGURE 2. (a) Optical image of an array of CVD graphene devices fabricated without a pinning dielectric. Following the metallization liftoff, rips, tears, and folds are visible in the devices. The Inset shows devices fabricated with a pinning dielectric, (b) Devices fabricated after HSQ pinning. Note the absence of tears and folds in the latter case.

Fig. 3 compares the Raman spectra of graphene devices after fabrication with that of pristine graphene. Upon fabrication of graphene devices, the D to G peak intensity ratio (I_D/I_G), which signifies the degree of disorder in graphene, increased from 0.08 to 0.56. Despite the increase in I_D/I_G ratio, the defect density in the fabricated graphene devices is still considered low [25], [26]. The point defect density in graphene can be quantified as [27]:

$$n_D\left(cm^{-2}\right) = \frac{(1.8 \pm 0.5) \times 10^{22}}{\lambda_L^4}\left(\frac{I_D}{I_G}\right), \tag{3}$$

where λ_L is the excitation laser wavelength (in nanometers). From equation (3) and using an excitation wavelength of 488 nm, n_D for pristine and fabricated graphene are 2.65×10^{10} cm^{-2} and 1.76×10^{11} cm^{-2}, respectively.

The increase in the defect density is partially attributed to the compressive stress that HSQ exerts on graphene which can, in turn, create vacancies, dislocations, and/or dangling bonds. The presence of compressive stress is confirmed from the blue shift of the G-peak after device fabrication as shown in Fig. 3 where the G-peak is blue-shifted from 1583.2 cm^{-1} to 1592.8 cm^{-1}. Using a biaxial stress model, the G band stress coefficient is estimated to be 7.47 cm^{-1}/GPa [28]. Thus, the compressive stress on the fabricated graphene devices is calculated to be 1.29 GPa. This is the main reason why our reported mobility is still falling behind the theoretical limit of 40,000 cm^2/V.s. We believe that optimizing the e-beam dose during lithography would decrease the compressive stress on graphene since the dose determines the degree of HSQ cross-linking. However, a more detailed study is still needed.

IV. CONTROLLING THE ETCH RATE OF HSQ

HSQ must be effectively cleared to insure robust contacts are made to the graphene surface. We studied the etching of HSQ using different etchants, including fluoride-based etchants due to the similarity in the chemical structure between HSQ and SiO_2. Various concentrations of hydrofluoric acid (HF) were used: 199:1 H_2O:HF made from 199 parts H_2O and one part 49% HF, 149:1 H_2O:HF made from 149 parts

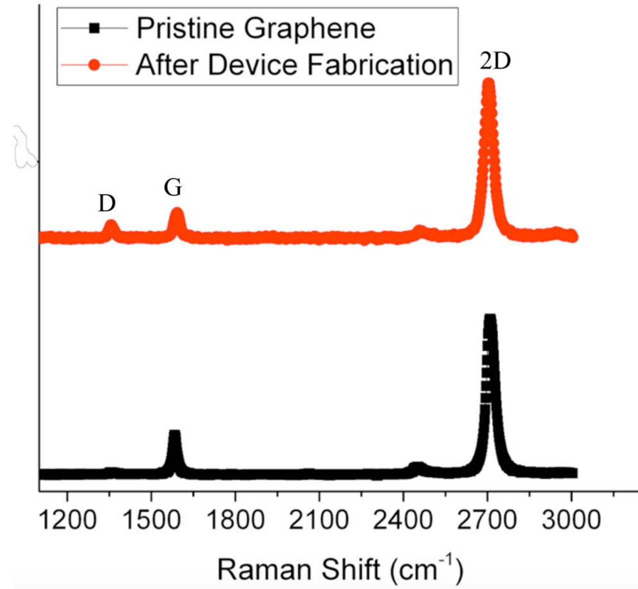

FIGURE 3. Raman spectra of graphene before and after device fabrication.

H_2O and one part 49% HF, 24:1 H_2O:HF made from 24 parts H_2O and one part 49% HF, 9:1 H_2O:HF made from 9 parts H_2O and one part 49% HF, 5:1 H_2O:HF made from 5 parts H_2O and one part 49% HF, and 6:1 Buffered Oxide Etch (BOE) made from 6 parts 40% NH_4F and one part HF. We also studied the size-dependency by patterning rectangles of sizes 200μm × 20μm, 400μm × 40μm, and 800μm × 80μm. To study the variability of the etching rate among the structure, we measured 20 samples from each size of the tested structures. HSQ was spin-coated on a degenerately p-doped Si substrate with a 300nm of thermally grown SiO_2 layer. Prior to the spin coating of HSQ, a thin Cr layer (100nm) is evaporated on SiO_2 which acts as a barrier layer and prevents the etchant from reaching the SiO_2 substrate, hence allowing for the accurate determination of the HSQ etch rate since SiO_2 is sensitive to fluoride-based etchants.

F^- based etchants effectively removed HSQ with an etching rate exceeding 40 nm/s for most of the concentrations studied. A low F^- ion concentration (less than 149:1 H_2O:HF) should be used if an accurate control of the etching process is required. Table 1 summarizes the etching rate of different etchants for 800μm × 80μm structures. It should be noted that the etch rate did not show a significant dependence on the pattern size with the etching rate being within 3% for all the studied sizes. 199:1 H_2O:HF has the lowest etching rate of 10.3 nm/s with a standard deviation of 1.3 nm/s; hence, this concentration should be used if an accurate control of the etching process is required. Higher F^- concentrations can be used if the etching process is not critical and a fast etching is needed. Table 1 also emphasizes the non-linear increase of the etching rate as a function of F^- ion concentration. Also the etching rate stayed constant at the beginning of the etching process then it drops down (Fig. 4). This is probably because the fresh surface of HSQ allows F^- ions to attack the Si ions in HSQ hence causing etching. Afterwards, a SiF layer is created on the surface of HSQ, which slows down the etching process.

TABLE 1. Etching rate of 800μm × 80μm HSQ structures for different F^- based etchants.

Etchant	Etching Rate (nm/s)	Standard Deviation (nm/s)
199:1 H_2O:HF	10.3	1.3
149:1 H_2O:HF	21.5	1.8
24:1 H_2O:HF	>40	-
6:1 BOE	>40	-

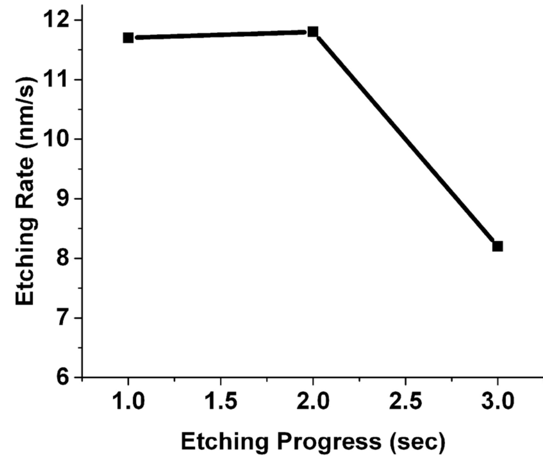

FIGURE 4. Progress of etching rate for 800μm × 80μm HSQ structures.

V. INTERCONNECT PERFORMANCE PROJECTIONS

To obtain the current in a graphene interconnect, Landauer formula can be used as [29]:

$$I = \frac{q}{h}\int_{-\infty}^{\infty} 2\sum_{m}\frac{l_{eff}}{L+l_{eff}}\left[f\left(E-\mu_1\right)-f\left(E-\mu_2\right)dE\right], \tag{4}$$

where h is Planck's constant, q is the elementary charge, L is the length of the interconnect, f is the Fermi distribution function, μ_1 and μ_2 are the electrical potential on each side of the graphene, E is the energy level, m is the number of subbands, assuming a semiconducting armchair graphene [30], and l_{eff} is the effective mean-free-path (MFP) of the graphene, which is extracted based on the analytical equation that is written as [31]:

$$MFP = \frac{\hbar}{q}\mu\sqrt{n\pi}, \tag{5}$$

where $\hbar$ is the reduced Planck's constant, μ is the mobility extracted from the experiment, n is the carrier concentration that is calculated by $n = \frac{\varepsilon_0\varepsilon_r}{t_{ox}}V_g$, and V_g is the applied back-gate voltage. The corresponding Fermi energy of the

graphene, E_F, can be obtained based on the model, shown as [32]:

$$E_F = \frac{1}{\gamma t_{ox}} \left(\sqrt{\varepsilon^2 + 2\gamma\varepsilon q V_g t_{ox}} - \varepsilon \right), \quad (6)$$

where $g = (4\pi q^2)/(h^2 v_F^2)$ is a constant depending on graphene properties, and $v_F = 10^6 m/s$ is the Fermi velocity.

Based on equations (3) - (6), the resistance calculated based on quantum transport theory match well with the experimentally measured data, shown in Fig. 5a, and Fig. 5b shows the extracted MFP at various carrier concentrations. This demonstrates the consistency of the simulation approaches used in this paper.

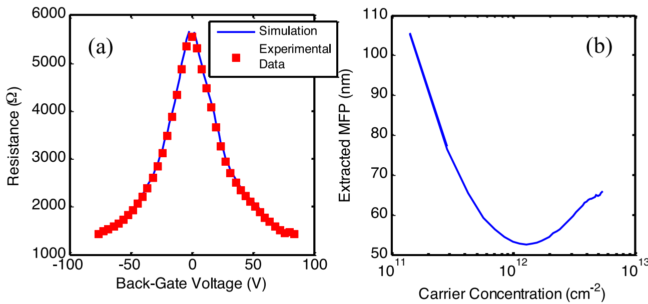

FIGURE 5. (a) Comparison between experimental measured resistance and simulation results based on extracted MFP values from the experiments for various back-gate voltages. (b) Extracted MFP versus carrier concentration.

Since the resistance per unit length of a single-layer graphene is much larger than that of a copper wire, multi-layer graphene interconnects are considered in this work. The fermi energy is chosen as 0.35eV. Previous work has shown both theoretically and experimentally that top contacts cannot fully utilize the potential benefits of multi-layer graphene interconnects because the current needs to be redistributed to other graphene layers through the interlayer resistance, which reduces the overall conductivity [33], [34]. Therefore, in this work, side contacts that electrically connect to all graphene layers are assumed to be possible. As the interconnect dimension scales down, the resistance per unit length of copper increases dramatically because of 1) the smaller cross-sectional area, 2) the severe size effects, and 3) the thick diffusion barrier that takes an ever-increasing fraction of the wire volume [35]. Therefore, we investigate the potential benefits of graphene interconnects at the sub-10nm dimensions at the end of ITRS [36]. The MFP of graphene is based on the experimentally extracted value in this work, assuming smooth edges. The capacitance value is estimated based on the quantum capacitance and the electrostatic capacitance, which is adopted from the previous work [37]. The contact resistance is 100 $\Omega \cdot \mu$m based on the previous experimental values [38].

The intrinsic interconnect energy-delay product versus the number of graphene layers is shown in Fig. 6. The interconnect width and length are 7 nm and 5 μm, respectively. Three different MFPs relative to the experimentally extracted value are explored and compared. In addition, two different edge smoothness are investigated, including perfect edge and edge scattering probability of 0.2, which is measured in the experiment [39].

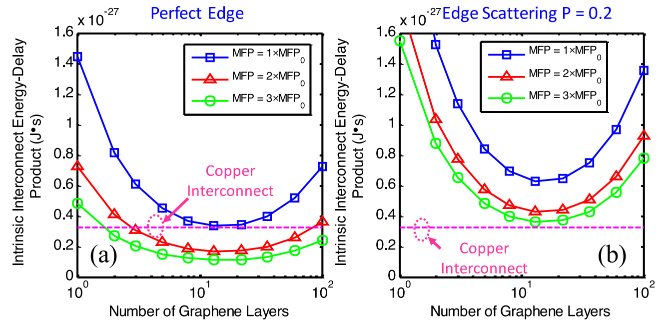

FIGURE 6. Intrinsic interconnect energy-delay product versus the number of graphene layers for various MFPs with (a) perfect edge and (b) edge scattering probability of 0.2.

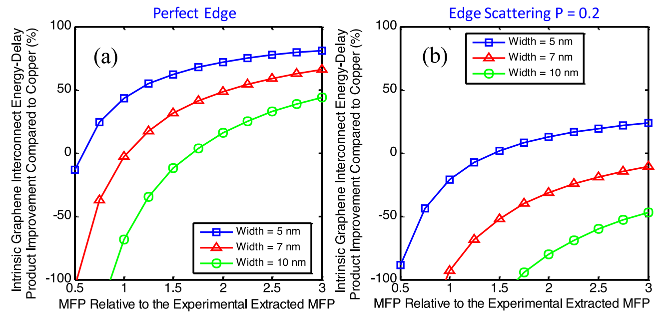

FIGURE 7. Intrinsic interconnect energy-delay product improvement versus the MFP of graphene for three different interconnect width with (a) perfect edge and (b) edge scattering probability of 0.2.

Optimal numbers of graphene layers exist to achieve the minimum intrinsic interconnect energy-delay product (EDP). This is because when the number of graphene layers is small, the large resistance of the graphene interconnect dominates the delay, and increasing the number of graphene layers significantly reduces the interconnect resistance. However, if there are too many graphene layers, the line-to-line capacitance increases significantly, overshadowing the benefits of the resistance saving. Therefore, the improvement starts to decrease when the number of layers is beyond a certain point. To achieve a comparable intrinsic delay with copper interconnects, the edge smoothness is crucial based on the comparison between Fig. 6a and 6b.

To explore the potential benefits of various hypothetical MFP relative to the experimentally extracted data, the percentage of the improvement in EDP compared to copper are investigated for three different wire width, shown in Fig. 7. The improvement increases at a narrow dimension as a result of the significant increase of the copper interconnect resistivity due to the size effect. If the MFP can be further improved, up to 80% of the EDP can be saved for a smooth graphene interconnect with 3× of the experimentally extracted MFP value at the width of 5nm. From Fig. 7b, the edge roughness

of the graphene significantly reduces its advantage over the copper interconnect, where at least 2× of the experimentally extracted MFP value is required for a 5 nm wide graphene interconnect to achieve a better EDP.

VI. CONCLUSION

In summary, we presented a simple two-step lithography process to fabricate graphene devices with record-breaking CVD graphene electron and hole mobilities of 25,600 and 23,700 cm^2 /Vs, respectively. The fabricated devices exhibit a high degree of symmetry between electron and hole conductions and had a minimum conductivity point very close to zero voltage, indicating minimal unintentional doping. The high quality of these devices is attributed to the presence of a HSQ pinning dielectric that is applied immediately after the transfer step. This dielectric anchors the loosely bound graphene sheet to the SiO_2 surfaces, primarily screening local charged impurities and secondarily reducing process damage. Peripheral process development with the spin-on glass, HSQ, was presented. F^- based etchants were shown to be very effective HSQ etchants with an etching rate that can exceed 40 nm/s. A low F^- ion concentration (less than 149:1 H_2O:HF) should be used if an accurate control of the etching process is required. The proposed fabrication method is expected to bring new focus to post-transfer passivation of CVD graphene as a means of improving quality and suppressing device-to-device variation. The potential benefits of graphene interconnects are evaluated based on the MFP extracted from the experimental data. Up to 80% of the EDP can be saved for a smooth graphene interconnect at the width of 5 nm if the MFP can reach 3× of the value in the experiment.

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